GX8006 Datasheet

High performance, Low-Power AI Voice Recognition Processor

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Document Revision History:

Version	Date	Change Log	Author
V1.0	2025.03.20	Initial version	

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1.Features

GX8006 is a high-performance, cost-optimized voice recognition and processing chip. It integrates a low-power Neural Processing Unit (NPU) , a 32-bit RISC-V CPU, ADC/DAC, and comprehensive peripheral suite.
The chip is capable of voice signal processing and offline voice recognition. It is an ideal solution for various AI-voice interaction applications due to its ease of use and performance.

CPU:

- 32-bit RISC-V CPU with Digital Signal Processor(DSP) and Floating-Point Unit(FPU) extensions
- 8KB I-Cache, 4KB D-Cache
- Maximum frequency 200MHz
- Supports various audio encoding and decoding

NPU:

- Integrated neural processor gxNPU V122, maximum operation frequency: 200MHz
- Supports 8/16-bit quantization and weights compression
- Supports Deep Neural Network(DNN), Convolutional Neural Network(CNN), Long Short-Term Memory(LSTM) and other popular neural network architectures
- Compilers support TensorFlow and PyTorch

Memory:

- Built-in SRAM, size 176KB
- System in Package(SIP) Quad Serial Peripheral Interface(QSPI) Nor Flash, size 2MB，maximum frequency 100MHz
- 256-bit One-Time Programmable(OTP) memory
- Supports external Pseudo Static Random Access Memory(PSRAM)

Audio ADC:

- Integrated 2 channel 16-bit audio ADCs
- Integrated PGA, supports 20~32dB gain with 2dB per step

Audio Out:

- Integrated high-performance audio output pipeline and DAC
- Integrated Class-D Power Amplifier (PA) delivering 1W output power at 5V into 8Ω / 4Ω load

Communication Interfaces:

- 3 Universal Asynchronous Receiver/Transmitter(UART) interfaces, one supporting flow control
- 1 I2C master and slave
- I2S input and output
- 6 Pulse Width Modulation(PWM) output ports

- Supports 1 QSPI master with eXecute In Place(XIP)
- 1 Serial Peripheral Interface(SPI) master and slave
- Infra-red transmitter and receiver
- 5V-tolerant General Purpose Inputs/Outputs(GPIOs) (P2 & P3)
- 6 Timers and watch dog timer

System Control:

- Integrated Power-On Reset(POR) and Brown-Out Reset(BOR)
- Internal 12MHz OSC and PLL
- No external crystal clock required

Voltage Supply:

- Single 3.0~5.5 V power supply
- Integrates Low Dropout Regulators(LDOs) for core and IO power supply

Package Type:

- SSOP-24

Quality:

- Temperature: -40~85℃

2.Chip Architecture

2.1.Block Diagram

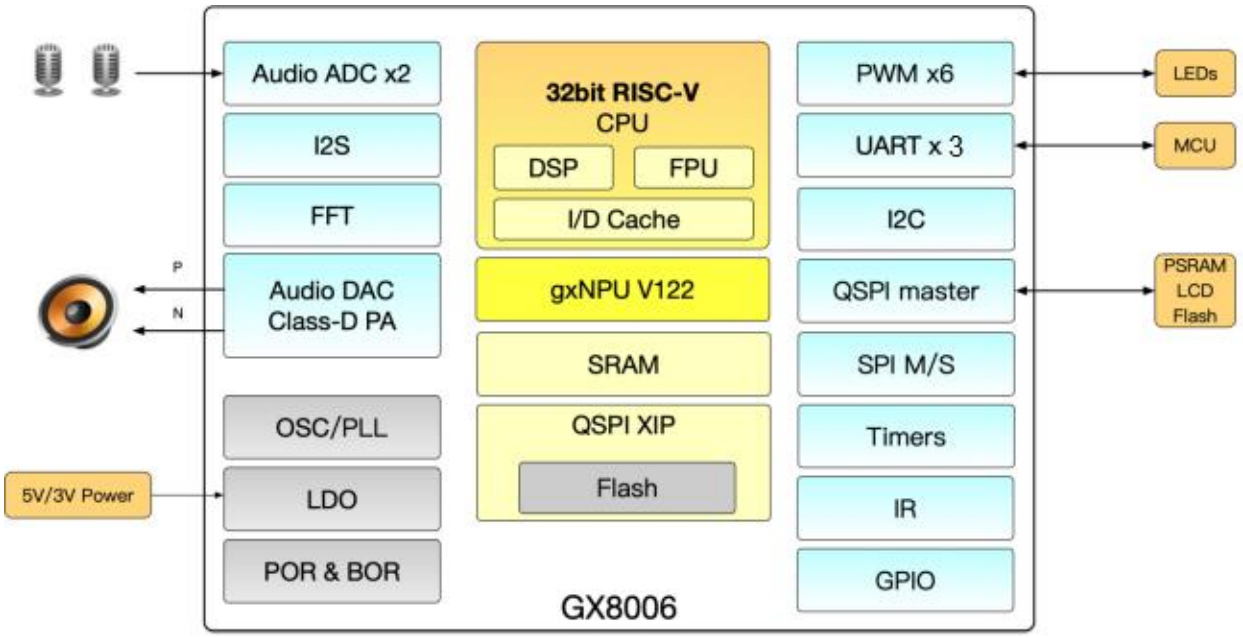


Figure 2- 1 GX8006 chip block diagram

3.Pin Description

3.1.Pin Map

GX8006 is available in 24-pin SSOP-24 package.

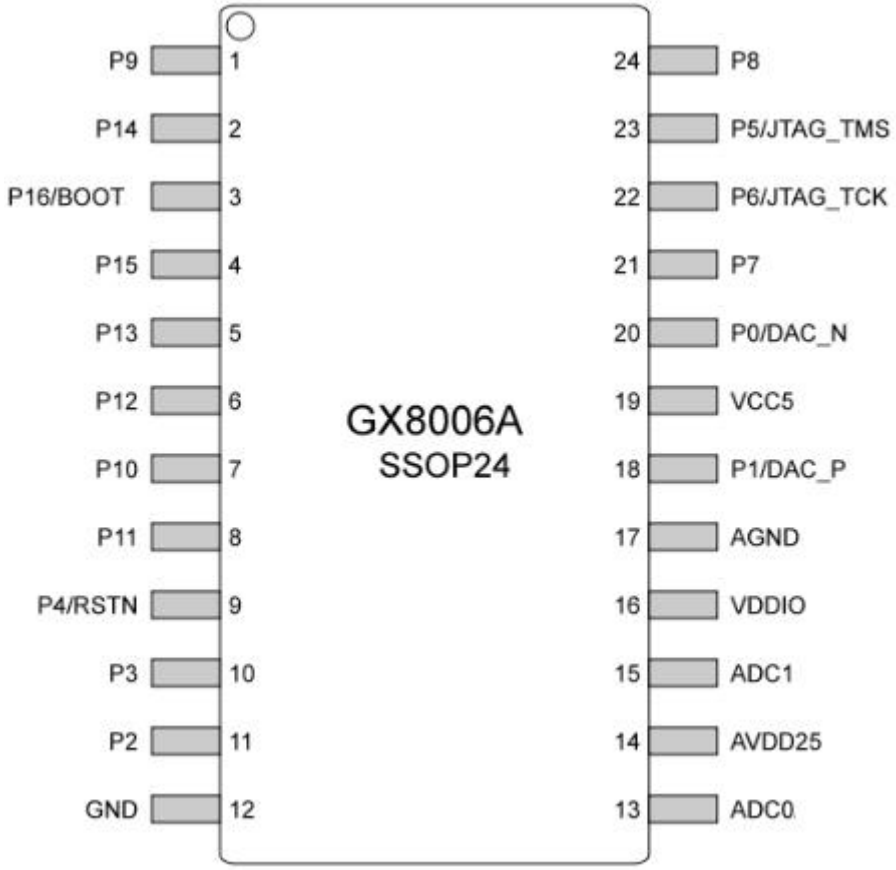


Figure 3- 1 GX8006 pin map

3.2.Pins Description

Table 3- 1 Pins Description

Pin Num	Pin Name	Type	Domain	Description
1	P9	Digital	VDDIO	MPIO P9
2	P14	Digital	VDDIO	MPIO P14
3	P16/BOOT	Digital	VDDIO	MPIO P16 share with BOOT ,*Note: During the boot stage, if the BOOT pin is pulled LOW, the device will automatically enter Flash Programming Mode
4	P15	Digital	VDDIO	MPIO P15
5	P13	Digital	VDDIO	MPIO P13
6	P12	Digital	VDDIO	MPIO P12
7	P10	Digital	VDDIO	MPIO P10
8	P11	Digital	VDDIO	MPIO P11
9	P4/RSTN	Digital	VDDIO	MPIO P4 share with RSTN
10	P3	Digital	VDDIO	MPIO P3 5V tolerant, and supports open-drain to 5V(VCC5) with external pull-up resistor
11	P2	Digital	VDDIO	MPIO P2 5V tolerant, and supports open-drain to 5V(VCC5) with external pull-up resistor
12	GND	Ground		GND
13	ADC0	Analog/Digital	AVDD25	Analog input of audio ADC0. *Note: ADC0 shall NOT Be Pulled Down
14	AVDD25	Power		Audio LDO OUTPUT, external capacitor required，2.5V
15	ADC1	Analog	AVDD25	ADC1 INPUT
16	VDDIO	Power		Digital IO power output, range 2.85~3.3V, maximum current 200mA, external capacitor required
17	AGND	Ground		Audio GND
18	P1/PA_P	Analog/Digital	VCC5	MPIO P1 and audio PA_P output, and supports open-drain to 3V(VDDIO) with external pull-up resistor
19	VCC5	Power		DC5V INPUT
20	P0/PA_N	Analog/Digital	VCC5	MPIO P0 and audio PA_N output，and supports open-drain to 3V(VDDIO) with external pull-up resistor
21	P7	Digital	VDDIO	MPIO P7
22	P6/JTAG_TCK	Digital	VDDIO	MPIO P6 share with JTAG_TCK
23	P5/JTAG_TMS	Digital	VDDIO	MPIO P5 share with JTAG_TMS
24	P8	Digital	VDDIO	MPIO P8

3.3.GPIO Pin Multiplexing Functions

Table 3- 2 Pin Multiplexing Functions

Pin	Pin Name	Function00	Function01	Function02	Function03	Function04	Function05	Function06	Function07
1	P9	IDLE (Hi-Z)	SPI2_MISO	UART2_CTS	PWM3	I2S_DOUT		IRC_RX	GPIO9
2	P14	IDLE (Hi-Z)	SPI2_MISO		PWM4	MSPI1_MISO	JTAG_TCK		GPIO14
3	P16/BOOT	BOOT with pull-up	I2S_MCLK	UART2_TX	PWM0	MSPI1_HOLD	I2C_SCL	IRC_RX	GPIO16
4	P15	IDLE (Hi-Z)	I2S_LR	UART2_RX	PWM5	MSPI1_WP	I2C_SDA	IRC_TX	GPIO15
5	P13	IDLE (Hi-Z)	SPI2_MOSI		PWM3	MSPI1_MOSI			GPIO13
6	P12	IDLE (Hi-Z)	SPI2_CLK		PWM2	MSPI1_CLK			GPIO12
7	P10	IDLE with pull-up	SPI2_MOSI	UART2_RTS	PWM4	I2S_LR	JTAG_TCK	IRC_EN	GPIO10
8	P11	IDLE (Hi-Z)	SPI2_CS		PWM1	MSPI1_CS			GPIO11
9	P4/RSTN	RSTN with pull-up				I2S_DIN	JTAG_TMS	IRC_EN	GPIO4
10	P3	IDLE with pull-up		UART0_TX	PWM3	JTAG_TCK	I2C_SCL	DAC_N	GPIO3
11	P2	IDLE with pull-up	I2S_DIN	UART0_RX	PWM2	JTAG_TMS	I2C_SDA	DAC_P	GPIO2
18	P1/DAC_P	IDLE (Hi-Z)	PA_P	UART1_RX	PWM1	I2S_BCLK	I2C_SCL	DAC_N	GPIO1
20	P0/DAC_N	IDLE (Hi-Z)	PA_N	UART1_TX	PWM0	I2S_DOUT/LR	I2C_SDA	DAC_P	GPIO0
21	P7	IDLE (Hi-Z)	SPI2_CLK	UART2_RX	PWM1	I2S_MCLK	I2C_SDA	IRC_RX	GPIO7
22	P6/JTAG_TCK	JTAG_TCK with pull-up		UART2_TX	PWM0	I2S_MCLK	I2C_SCL	IRC_EN	GPIO6
23	P5/JTAG_TMS	JTAG_TMS with Hi-Z	I2S_DIN	UART2_RX	PWM5	I2S_LR	I2C_SDA	IRC_TX	GPIO5
24	P8	IDLE (Hi-Z)	SPI2_CS	UART2_TX	PWM2	I2S_BCLK	I2C_SCL	IRC_TX	GPIO8

Note: **IDLE**: High impedance, no function

4.Function Overview

4.1.CPU Architecture

- 32-bit RISC-V CPU, maximum frequency 200MHz
- 8KB I-Cache，4KB D-Cache
- Supports DSP and FPU acceleration unit

4.2.Memory

- Integrated 176KB SRAM
- Internally encapsulates 2MB SPI NOR flash in SIP style
  - Supports standard, dual or quad mode of SPI interface
  - Allow to XIP directly from flash
  - SPI clock frequency up to 120MHz

4.3.Clock

- On-chip12MHz oscillator circuit
- One phase-locked loops (PLL)

4.4.NPU

- NationalChip's gxNPU V122
- Supports DNN/CNN/LSTM and other popular neural network architectures
- Supports 8/16 bit quantization, and weights compression
- Compilers support direct conversion from TensorFlow and PyTorch

4.5.Audio

- Integrated 2 channel 16-bit audio ADCs, supports sample rate of 16KHz
- Integrated PGA, supports 20~32dB gain with 2dB per step
- Integrated high-performance audio output pipeline and DAC
- Integrated Class-D PA delivering 1W output power at 5V into 8Ω / 4Ω load
- Integrated I2S interface, supports input and output, supports Master and Slave mode

4.6.System Peripheral

- I2C
  - Integrated one I2C controller
  - Master or Slave Mode
  - Supports speed 100KHz，400KHz and up to **1MHz (P2 & P3 port only, with VDDIO = 3V)**

- DMA
  - 3 channel DMA
  - Supports 8/16/32-bit data width
  - Supports memory-to-memory, memory-to-peripheral, and peripheral-to-memory data transfer types

- UART
  - Integrated 3 UART interfaces
  - Full-duplex operation
  - Supports speed up to 1.5 Mbps
  - Uart2 Supports flow control function

- Timer
  - Consists of four 32-bit up-counters
  - Integrated RTC timers

- WDT
  - Programmable and hard coded reset pulse length
  - An interrupt is generated first, and if the interrupt is not cleared by the service routine before the second timeout, a system reset is generated
  - 32-bit Watchdog Timer(WDT) counter

4.7.Power Management

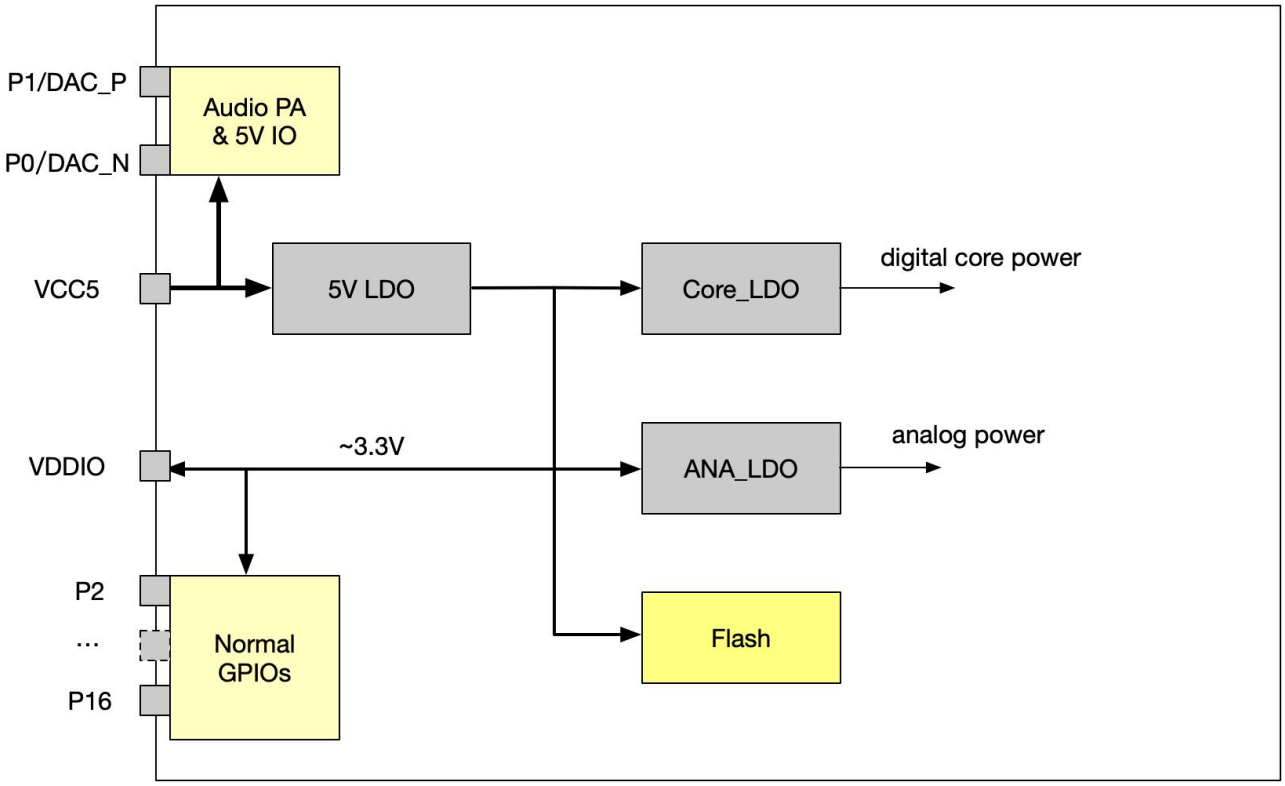


Figure 4- 1 Chip power supply system

- VCC 5V input range: 3.0V~5.5V [1]
- VDD IO output range: 2.7V~3.3V

1*,*Note:

①. When VCC5=[3.6V~5.5V]，LDOIO must be in work mode, and VDDIO can be configured to 3V/3.3V.

②. When VCC5=[3.3V~3.6V)，LDOIO must be in work mode, and VDDIO can be configured to 3V only.

③. When VCC5=[3.0V~3.3V)，LDOIO must be in bypass mode，and VDDIO=VCC5.

4.8.POR and BOR

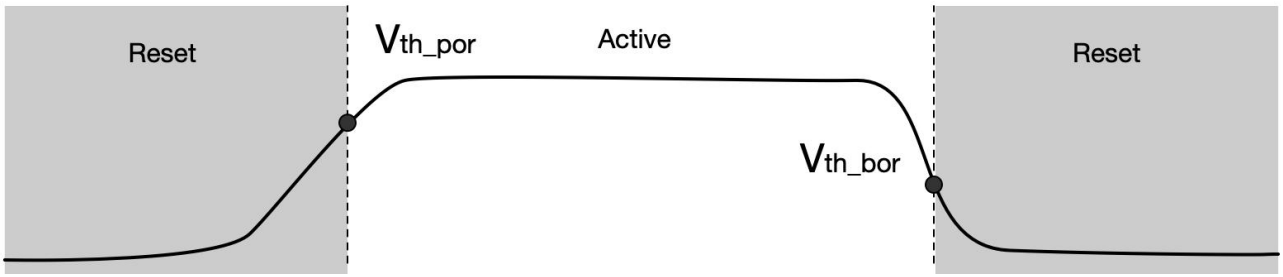


Figure 4- 2 Power on reset and brown out reset

Table 4-1 POR and BOR threshold

Parameter	Description	MIN	TPY	Max	Unit
Vth_por	VCC5 voltage > Vth_por, reset release.	2.6	2.8	3.0	V
Vth_bor	VCC5 voltage < Vth bor, will enter reset mode.	2.4	2.6	2.8	V

5.Applications

5.1.Typical Applications

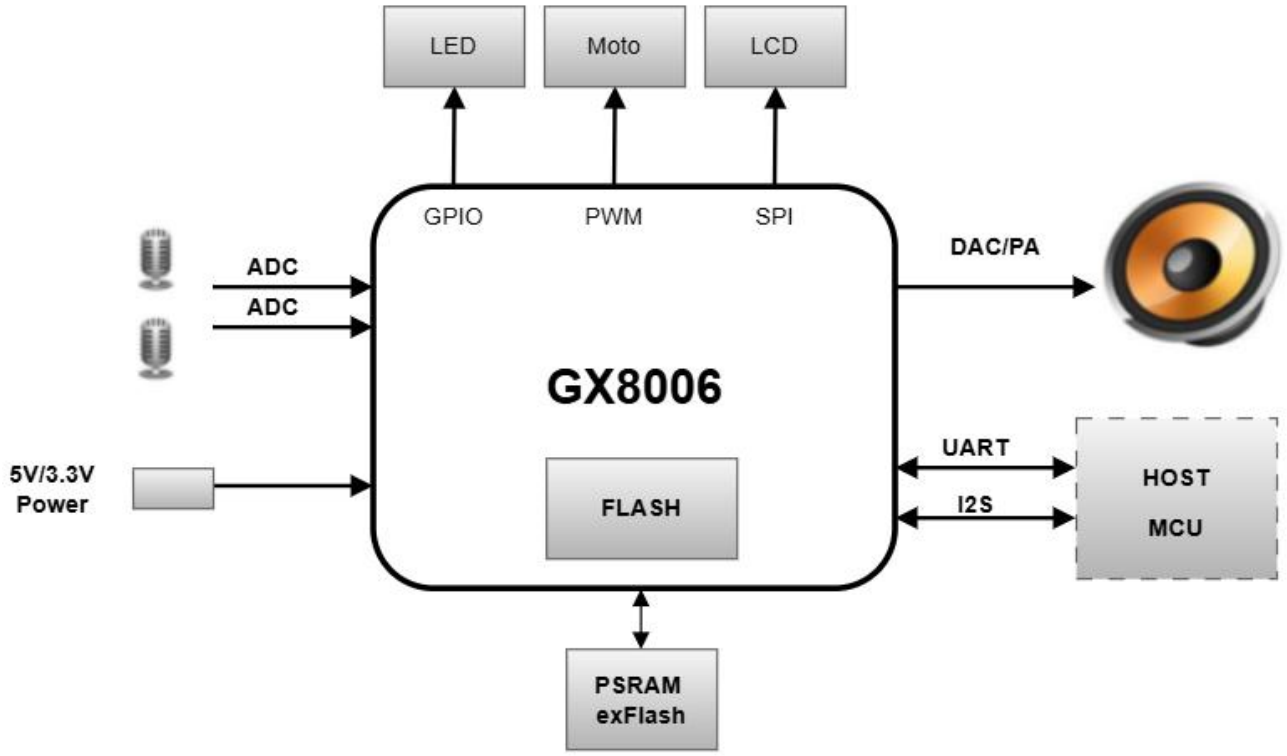


Figure 5- 1 Block diagram of voice enabled IOT device

Key Features:

- Two Analog microphone inputs
- Supports 1+1 AEC or 2 Mic array
- Direct connect to speaker with Class-D PA delivering 1W output power at 5V into 8Ω / 4Ω load
- Single power supply from 3.0V to 5.5V
- AI voice recognition, voice key word detection, voice commands recognition
- AI denoising, Beamforming(BF), Direction of Arrival(DOA), and etc

5.2.Recommended Operating Condition

Table 5- 1 Recommended operating conditions

Parameters	Min	Typ	Max	Unit
Power supply voltage(VCC5)	3.0	5	5.5	V
IO Power output Voltage(VDDIO)	2.7	3	3.3	V
Output High Level (VOH) for IO(except P0&P1)	2.7	3	3.3	V
Output High Level (VOH) for P0 & P1	3.6	5	5.5	V
Output Low Level (VOL) for P0 & P1		0	0.4	V
Input High Level (VIH) for P0, P1, P2 & P3	2.0		5.5	V
Input High Level (VIH) for other GPIO	2.0		3.3	V
Input Low Level (VIL)	-0.3		0.8	V
Pull-up Resistor for IO(except P0&P1)	27K	40K	65K	Ω
Pull-down Resistor for IO(except P0&P1)	33K		87K	Ω
Pull-up Resistor for P0 & P1		6K		Ω
Pull-down Resistor for P0 & P1		6K		Ω

Table 5- 2 Recommended operating conditions continue

Parameters	Min	Typ	Max	Unit	Remark
Storage Temperature	-40	25	150	℃	
Operating Ambient Temperature	-40	25	85	℃	

5.3.Electrostatic Discharge

Table 5- 3 Electrostatic discharge

Parameters	Min	Max	Unit
Human Body Model (HBM)	-4	4	kV
CDM	-1000	1000	V

6.Electronic Specification

6.1.ADC Characteristics

Table 6-1 ADC performance testing report

＊all specifications at T= 25℃, VCC5= 5V, AVDD25= 2.5V, ADC_GAIN= 6dB, single-ended input

Parameter	Test condition	Min	Typ	Max	Unit
Input Common Mode	AVDD25/2	-	1.25	-	V
Pga_Gain		-	0~32	-	dB
Full Scale Input Voltage	(THD+N=0.2%)	-	2.47	-	Vpp
Noise	Fs=16KHz A-weighted	-	-81	-	dBFS
SNR	Fs=16KHz A-weighted	-	80	-	dB
Dynamic Range	4.4mVpp input (-60dB of max input level) Fs=16KHz A-weighted	-	78	-	dB
THD	Best at -6dBFS input Fs=16KHz A-weighted	-	-73	-	dB
Current	ADC+PGA+LDO	-	2.83	-	mA

6.2.DAC Characteristics

Table 6- 2 DAC performance testing report

＊all specifications at T= 25℃, VCC5= 5V

Parameter	Min	Typ	Max	Unit	Test condition
Output Swing	–	5.9	–	dBu	Input 0dBFs **Single ended mode**
	–	1.52	–	Vrms	
Noise	–	-63	–	dBu	
SNR	–	68.5	–	dB	
THD+N	–	-52.9	–	dB	
Output Swing	–	4.76	–	dBu	Input 0dBFs **Differential mode**
	–	1.34	–	Vrms	
Noise	–	-76	–	dBu	
SNR	–	81	–	dB	
THD+N	–	-53	–	dB	

6.3.PA Characteristics

Table 6- 3 PA performance testing report (RL = 8Ω)

＊all specifications at T= 25℃, VCC5= 5V，PA output load= 8Ω

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Power Voltage	VCC5		3	5	5.5	V
Quiescent Current	IDD	VIN=0V，VCC5 = 5V，No Load		19		mA
Sampling Frequency	Fsw	VCC5 = 3.0V to 5.25V		24.576		MHz
Output Power	PO	THD+N=1%，f=1KHz,VCC5=5V		1		W
		RL=8 Ω (VCC5 CAP=100uF)				
		THD+N=3%，f=1KHz,VCC5=5V		1		W
		RL=8 Ω (VCC5 CAP=1uF)				
		THD+N=10%，f=1KHz,VCC5=5V		1.15		W
		RL=8 Ω (VCC5 CAP=100uF)				
		THD+N=10%，f=1KHz,VCC5=5V		1.1		W
		RL=8 Ω (VCC5 CAP=1uF)				
Total Distortion+Noise	THD+N	VCC5=5V，f=1KHz	-	0.8		%
		RL=8 Ω，Po=0.5W (VCC5 CAP=100uF)				
		VCC5=5V，f=1KHz		1.3		%
		RL=8 Ω，Po=0.5W (VCC5 CAP=1uF)				

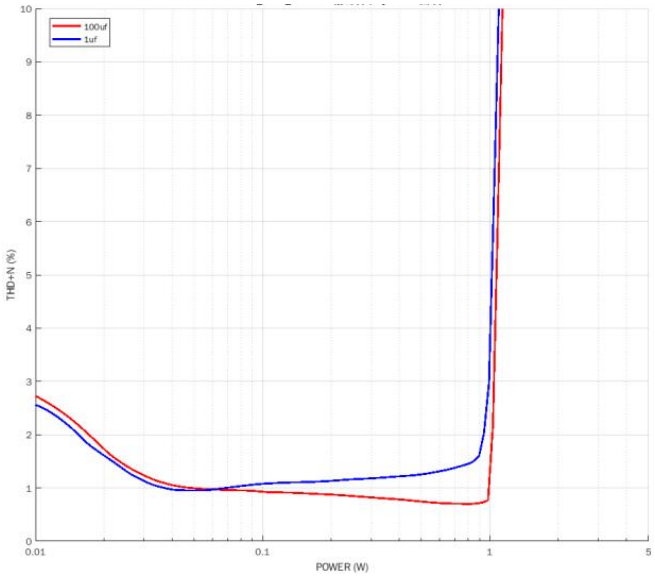


Figure 6- 1 THD+N vs Output Power (RL = 8 Ω)

Table 6-4 PA performance testing report (RL = 4Ω)

＊all specifications at T= 25℃, VCC5= 5V，PA output load= 4Ω

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Power Voltage	VCC5		3	5	5.5	V
Quiescent Current	IDD	VIN=0V，VCC5 = 5V，No Load		19		mA
Sampling Frequency	Fsw	VCC5 = 3.0V to 5.25V		24.576		MHz
Output Power	PO	THD+N=1.5%，f=1KHz,VCC5=5V		1		W
		RL=4 Ω (VCC5 CAP=100uF)				
		THD+N=1.5%，f=1KHz,VCC5=5V		1		W
		RL=4 Ω (VCC5 CAP=1uF)				
		THD+N=10%，f=1KHz,VCC5=5V		1.65		W
		RL=4 Ω (VCC5 CAP=100uF)				
		THD+N=10%，f=1KHz,VCC5=5V		1.65		W
		RL=4 Ω (VCC5 CAP=1uF)				
Total Distortion+Noise	THD+N	VCC5=5V，f=1KHz	-	1.3		%
		RL=4 Ω，Po=0.5W (VCC5 CAP=100uF)				
		VCC5=5V，f=1KHz		1.3		%
		RL=8 Ω，Po=0.5W (VCC5 CAP=1uF)				

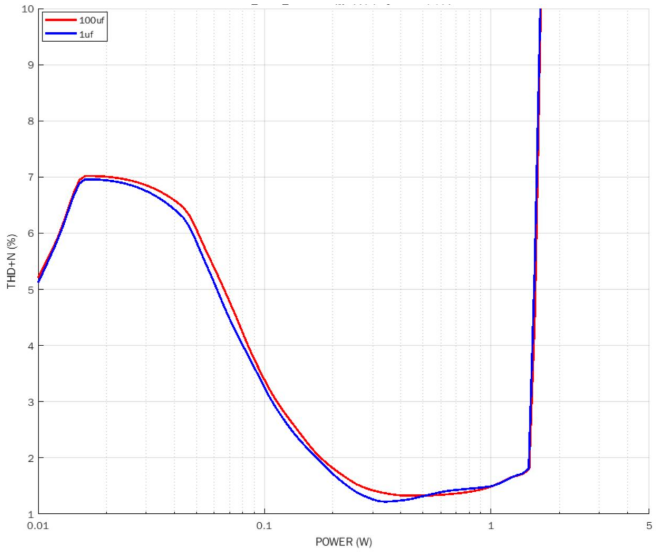


Figure 6-2 THD+N vs Output Power (RL = 4 Ω)

6.4.PMU Characteristics

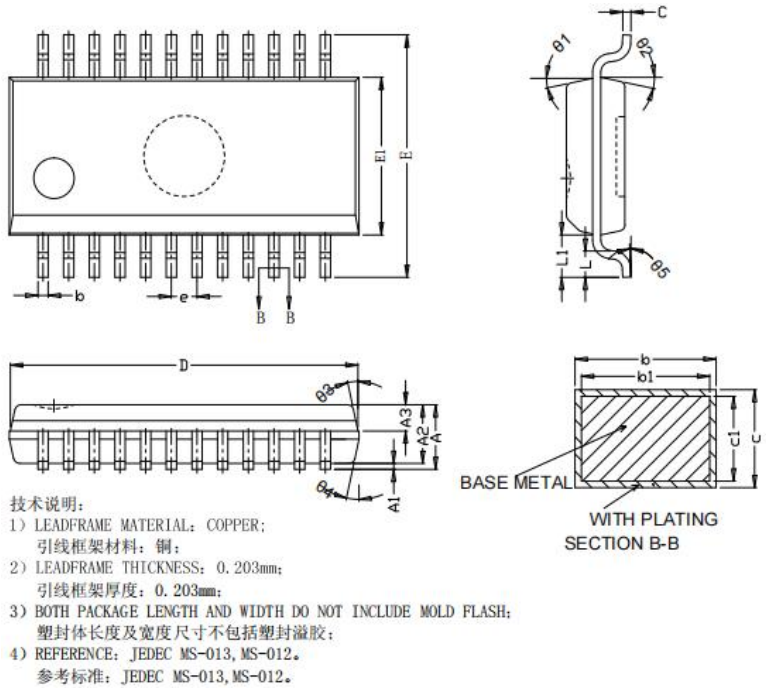
Table 6- 5 PMU performance testing report

＊all specifications at T= 25℃

Symbol	Description	Min	Typ	Max	Unit
VCC5 Input voltage	Input Voltage. PA Supply Voltage. P0&P1 IO Voltage	3.0	5	5.5	V
VDDIO Output Voltage	Internal LDO-IO output. IO Voltage(except P0 & P1). Analog supply voltage	2.7	3	3.3	V
VDDIO Output Current	Internal LDO-IO Loading current		200		mA

7.Package Information

7.1.Package Specification



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.70
A1	0.10	0.15	0.21
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.20	--	0.29
b1	0.20	0.24	0.27
c	0.18	--	0.23
c1	0.16	0.19	0.21
D	8.45	8.60	8.75
E	5.80	6.00	6.20
E1	3.75	3.85	3.90
e	0.635(BSC)		
L	0.58	0.60	0.63
L1	1.05(BSC)		
θ1	8°	~	15°
θ2	8°	~	15°
θ3	8°	~	15°
θ4	8°	~	15°
θ5	0°	~	6°

Figure 7- 1 SSOP-24 package specification

7.2.Chip Mark Description

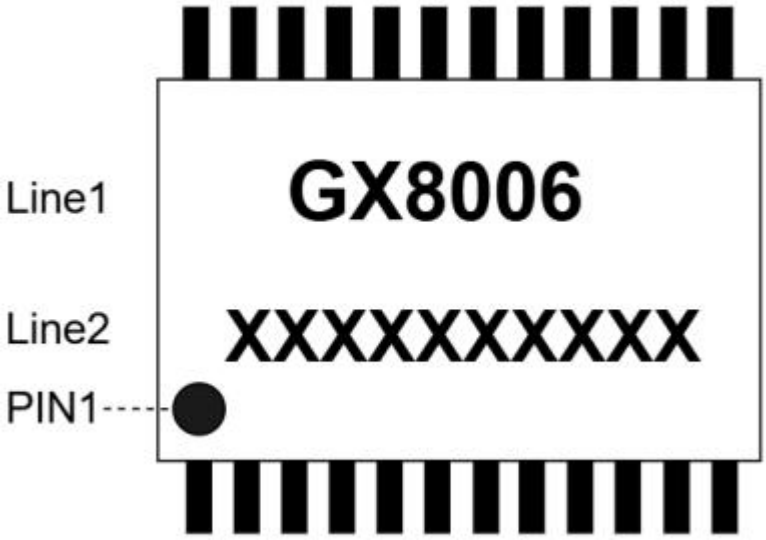


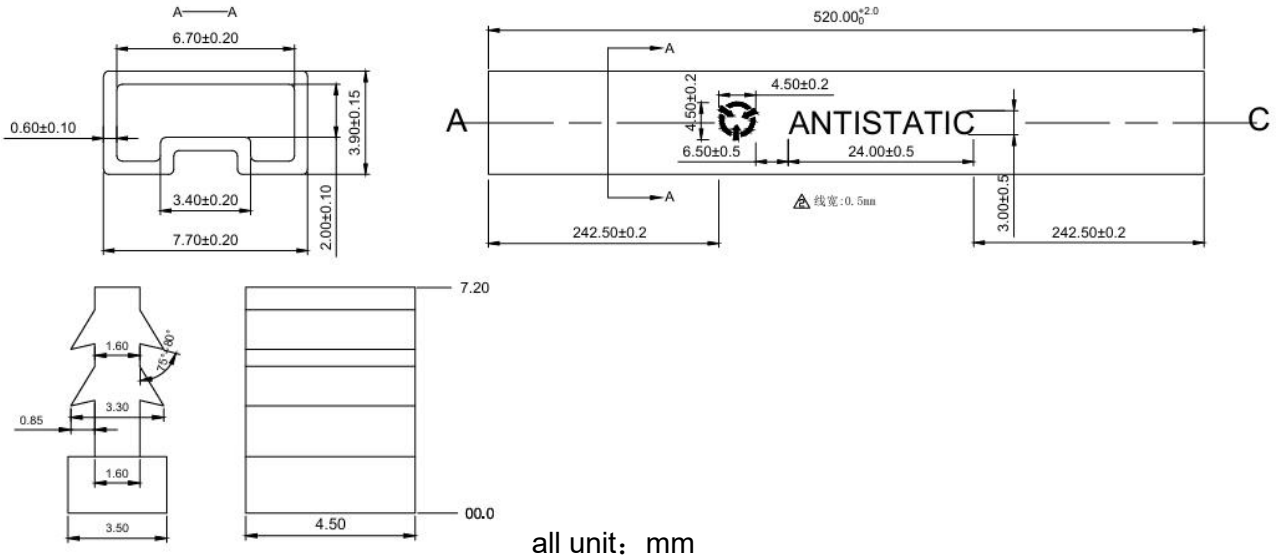
Figure 7-2 Chip mark description

Description:

- Line 1: Chip name
- Line 2: 10 digit of production lot number
- PIN 1: Pin 1 start point mark

7.3.TUBE Specification

1.TUBE Information



all unit：mm

Figure 7-3 TUBE information

7.4.Convection Reflow Profile

The test results comply with three-stage reflow soldering requirements, with a reflow temperature of 260℃. The details are as follows:

Table 7- 1 Convection reflow profile

Profile Feature	Note	Pb-Free Assembly
Average ramp-up rate	T_{smax} to T_p	0.6~1.5℃/sec
Preheat	-Temperature Min(T_{smin})	150℃
	-Temperature Max(T_{smax})	200℃
	-Time(min to max)(ts)	60-120sec
Time maintained above:	-Temperature(T_L)	217℃
	-Time(t_L)	60-150 sec
Peak Temperature(Tp)		250±5℃
Time within 5℃ of actual Peak Temperature(tp)		≥30sec
Ramp-down Rate		≤3℃/ sec
Time 25℃ to Peak Temperature		≤8 min

8.Ordering Information

Table 8- 1 Ordering information

Ordering Code	Embedded SPI Nor Flash	Package	MOQ
GX8006A	2MByte	SSOP-24	5k

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