GX8008

Smart voice front-end chip

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Application and Technical Information

For questions or comments pertaining to technical information, questions, and applications, please contact one of the following sales offices nearest you.

Sales Offices

Headquarters: (Hangzhou office in Zhejiang province, China)

Tel: +86-571-88156088-8858

South China: (Shenzhen office in Guangdong province)

Tel: +86-755-61637134

Southwest China: (Chengdu office in Sichuan province)

Tel: +86-28-61348936

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1. General Introduction

GX8008 is an embedded SoC chip designed for smart voice front-end applications. Targeted at the features of smart voice applications, GX8008 is uniquely designed in a heterogeneous multi-core architecture, which integrates self-developed Neural Process Unit (NPU), DSP for voice processing, 32bit RISC CPU, Audio DAC and other peripherals. It enables the product to perform deep neural network computation and various microphone array based on voice signal processing in chip. The chip integrates multi-channel ADC, audio DAC, rich peripheral interfaces as well as an embedded SRAM, which makes its size smaller, power consumption lower, and the entire hardware design simpler.

The highlights of the chip include following features:

- **NPU**: neural process unit that enables chipset to run deep learning model locally
- **CPU**: 32bit RISC CPU, frequency up to 150MHz, support JTAG
- **DSP**: Tensilica HIFI4 DSP processor, speed up to 400MHz
- **Mic Array**: support 6 analog or digital mic, both PDM and I2S are supported
- **Audio**: support analog and digital audio input and direct DAC output
- **Peripherals**: SPI master, I2C, UART, PWM, USB 2.0 Slave
- **Package**: QFN88, 10x10mm

2. Chip Architecture

2.1. Block Diagram

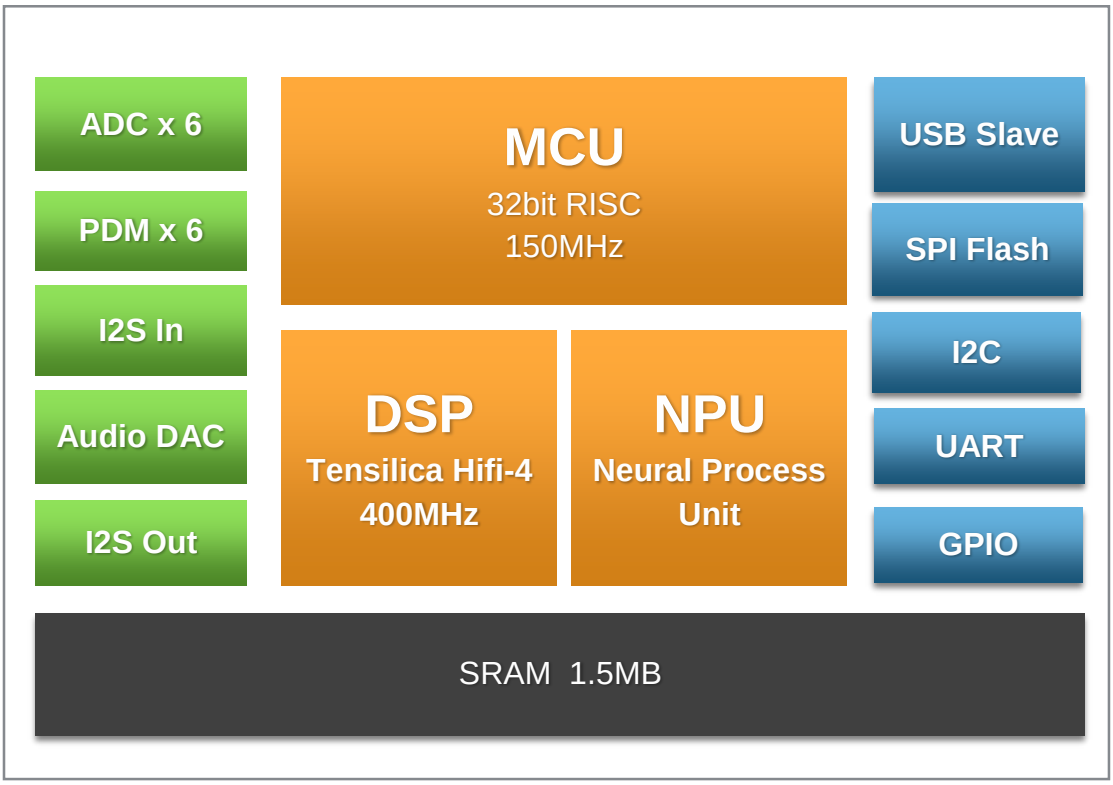


Figure 2-1 GX8008 Chip Block Diagram

The GX8008 chipset is designed for smart voice front-end system. It has an MCU for system booting, general task management and user applications. A high-performance DSP is built in for smart voice processing like VAD, de-noise, AEC, beamforming,etc. Also a powerful and efficient Neural Process Unit is designed for local deep learning model inference which can be used as voice keyword recognition or other similar tasks. As a front-end chip, GX8008 has various audio interfaces such as ADC, PDM,I2S and USB slave.The chip receives multi-channel microphone signals, and then does signal process and keywords spotting , and after that the data will transfer to host system by USB slave or other interfaces.

3. Feature List

- **DSP**:
    - Cadence Tensilica HIFI-4 voice and audio DSP, frequency up to 400MHz
    - Quad 32-bit MAC, eight 16-bit MAC
    - 32KB Instruction Cache, 32KB Data Cache
    - 32KB DTCM, 32KB PTCM
    - Support JTAG
- **NPU**:
    - Neural process unit dedicated for keywords spotting
    - 32 MAC, support DNN/CNN/LSTM and other classic models.
- **MCU**:
    - 32bit RISC MCU, frequency up to 150MHz
    - System booting and low power standby control
    - Coordinate the work flow of DSP, sNPU and the main CPU
- **Digital Mic Input:**
    - Support maximum 6 channel digital mic signal input
    - Support I2S and PDM
- **Analog Mic Input:**
    - Integrate 16-bit 6 channel Sigma-Delta ADC
    - Sample rate: 8KHz, 16KHz, 48KHz
    - Integrate PGA amplifier for each channel, 2dB per step.
    - SNR: 85dB
- **Audio Output:**
    - Dual channel 16-bit DAC with up to 95dB SNR
    - SPDIF and I2S output
    - USB 2.0 full speed slave mode, support linux UAC（USB Audio Class）

4. Pin Map

4.1. Pin Map

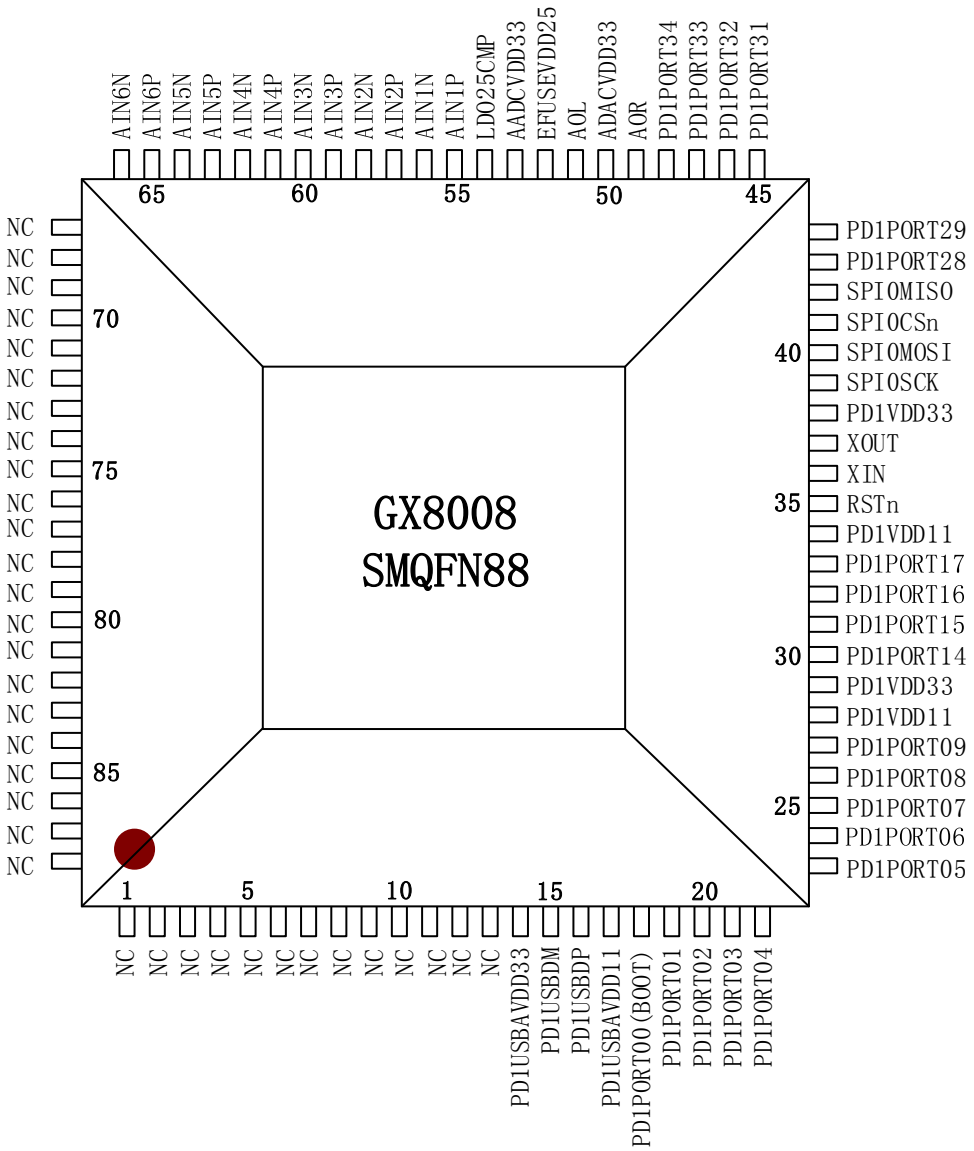


Figure 4-1 GX8008 Pin map

4.2. Acronyms

DP => Digital Power	DG => Digital Ground
AP => Analog Power	AG => Analog Ground
AI => Analog Input	AO => Analog Output
I => Digital Input	O => Digital Output
IO => Digital Bi-directional	AB => Analog Bi-directional

4.3. Pin Mux

Table 4-1 Pin Mux

PORT_NAME	PULL	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3	FUNCTION4	FUNCTION5
PD1PORT00	UP	GPIO0					
PD1PORT01		POWER_DOWN	GPIO1				
PD1PORT02	UP	UART0_RX	GPIO2				
PD1PORT03		UART0_TX	GPIO3				
PD1PORT04		OTP_AVDD_EN	GPIO4				
PD1PORT05	UP	SDBGTDI	DDBGTDI	SNDBGTDI	GPIO5		
PD1PORT06		SDBGTDO	DDBGTDO	SNDBGTDO	GPIO6		
PD1PORT07	UP	SDBGTMS	DDBGTMS	SNDBGTMS	PCM1INBCLK	GPIO7	
PD1PORT08	UP	SDBGTCK	DDBGTCK	SNDBGTCK	PCM1INLRCK	GPIO8	
PD1PORT09	UP	SDBGTRST	DDBGTRST	SNBGTRST	PCM1INDAT0	GPIO9	
PD1PORT14		PCMOUTMCLK	DUART_TX	GPIO14			
PD1PORT15		PCMOUTDAT0	SPDIF	GPIO15			
PD1PORT16		PCMOUTLRCK	GPIO16				
PD1PORT17		PCMOUTBCLK	GPIO17				
PD1PORT28	UP	SDA1	GPIO28				
PD1PORT29	UP	SCL1	GPIO29				
PD1PORT31	UP	PCM0INDAT0	PDMDAT2	GPIO31			
PD1PORT32		PCM0INMCLK	PDMDAT1	GPIO32			
PD1PORT33	UP	PCM0INLRCK	PDMDAT0	PCM0OUTLRCK	GPIO33		
PD1PORT34	UP	PCM0INBCLK	PDMCLK	PCM0OUTBCLK	GPIO34		
SPI0SCK		SPI0SCK					
SPI0MOSI	UP	SPI0MOSI					
SPI0CSn	UP	SPI0CSn					
SPI0MISO	UP	SPI0MISO					

4.4. Power and Ground Pins

Table 4-2 Power and Ground Pins

Pin Number	Signal	Type	Description
29,38	PD1VDD33	DP	3.3V digital power for IO
28,34	PD1VDD11	DP	1.1V digital power for core
50	ADACVDD33	AP	Power (3.3V) for Audio DAC
52	EFUSE2.5	AP	Power (2.5V) for EFUSE
53	AADCVDD33	AP	Power (3.3V) for Audio ADC
54	LDO25CMP	AP	Power (2.5V) for ADC power compensate
14	PD1USBVDD33	AP	Power (3.3V) for USB Slave
17	PD1USBVDD11	AP	Power (1.1V) for USB Slave

4.5. System Operation Signals

Table 4-3 System Operation Pins

Pin Number	Signal	Type	Description
36	XIN	I	Clock input or crystal input
37	XOUT	O	Output for crystal connection
35	RSTn	I	System reset, active low

4.6. ADC Interface Signals

Table 4-4 ADC Interface Signal Pins

Pin Number	Signal	Type	Description
55	ADCIN1_P	AI	Differential Voltage Inputs, Channel 1

Pin Number	Signal	Type	Description
56	ADCIN1_N	AI	Differential Voltage Inputs, Channel 1
57	ADCIN2_P	AI	Differential Voltage Inputs, Channel 2
58	ADCIN2_N	AI	Differential Voltage Inputs, Channel 2
59	ADCIN3_P	AI	Differential Voltage Inputs, Channel 3
60	ADCIN3_N	AI	Differential Voltage Inputs, Channel 3
61	ADCIN4_P	AI	Differential Voltage Inputs, Channel 4
62	ADCIN4_N	AI	Differential Voltage Inputs, Channel 4
63	ADCIN5_P	AI	Differential Voltage Inputs, Channel 5
64	ADCIN5_N	AI	Differential Voltage Inputs, Channel 5
65	ADCIN6_P	AI	Differential Voltage Inputs, Channel 6
66	ADCIN6_N	AI	Differential Voltage Inputs, Channel 6

4.7. SPI Flash Signals

Table 4-5 FLASH Signals

Pin Number	Signal	Type	Description
39	SPISCK	O	SCK of SPI interface
40	SPIMOSI	O	MOSI of SPI interface
41	SPICSn	O	CS of SPI interface
42	SPIMISO	I	MISO of SPI interface

4.8. Audio Play Interface Signals

Table 4-6 Audio play Interface Signals

Pin Number	Signal	Type	Description
49	AOR	AO	Audio DAC right channel output
51	AOL	AO	Audio DAC left channel output
30	PCMOUTMCLK	O	0: mclk of audio out i2s interface
	DUARTTX	O	1: DSP UART data transmit
	SNUARTTX	O	2: SNPU UART data transmit
	PD1PORT14	IO	3: Domain1 GPIO 14
31	PCMOUTDAT	O	0: data of audio out i2s interface
	SPDIF	O	1: Sony/Philips Digital Interface Format
	PD1PORT15	IO	2: Domain1 GPIO 15
32	PCMOUTLRCK	O	0: lrck of audio out i2s interface
	PD1PORT16	IO	1: Domain1 GPIO 16
33	PCMOUTBCLK	O	0: bclk of audio out i2s interface
	PD1PORT17	IO	1: Domain1 GPIO 17

4.9. Communication Interface Signals

Table 4-7 Communication Interface Signals

Pin Number	Signal	Type	Description
43	SDA1	IO	0: Data of I2C 1
	PD1PORT28	IO	1: Domain1 GPIO 28

Pin Number	Signal	Type	Description
44	SCL1	IO	0: Clock of I2C 1
	PD1PORT29	IO	1: Domain1 GPIO 29
22	PD1PORT04	IO	0: Domain1 GPIO 04
21	UART0TX	O	0: UART0 data transmit
	PD1PORT03	IO	1: Domain1 GPIO 03
20	UART0RX	I	0:UART0 data receive
	PD1PORT02	IO	1: Domain1 GPIO 02
19	POWER_DOWN	O	0: Domain 1 Power_down Controller
	PD1PORT01	IO	1: Domain1 GPIO 01
18	BOOT	I	0: Boot key
	PD1PORT00	IO	1: Domain1 GPIO 00

4.10.Audio In Interface Signals

Table 4-8 Audio In Interface Signals

Pin Number	Signal	Type	Description
45	PCM0INDAT0	I	0: data0 of audio in0 i2s interface
	PDMDAT2	I	1: data2 of audio in pdm interface
	PD1PORT31	IO	2: Domain1 GPIO 31
46	PCM0INMCLK	I	0: mclk of audio in0 i2s interface
	PDMDAT1	I	1: data1 of audio in pdm interface

Pin Number	Signal	Type	Description
	PD1PORT32	IO	2: Domain1 GPIO 32
47	PCM0INLRCK	I	0: lrlk of audio in0 i2s interface
	PDMDAT0	O	1: data0 of audio in pdm interface
	PCM0OUTLRCK	O	2: lrck of audio out i2s interface from core
	PD1PORT33	IO	3: Domain1 GPIO 33
48	PCM0INBCLK	I	0: bclk of audio in0 i2s interface
	PDMCLK	O	1: mclk of audio in pdm interface
	PCM0OUTBCLK	O	2: bclk of audio out i2s interface from core
	PD1PORT34	IO	3: Domain1 GPIO 34

4.11.USB Interface Signals

Table 4-9 USB Interface Signals

Pin Number	Signal	Type	Description
16	USBDP	AB	USB Slave Data pin Data+
15	USBDM	AB	USB Slave Data pin Data-

4.12.JTAG Interface Signals

Table 4-10 JTAG Interface Signals

Pin number	Signal	Type	Description
23	SDBGTDI	I	0: SCPU Debug interface data input
	DDBGTDI	I	1: DSP Debug interface data input

Pin number	Signal	Type	Description
	SNDBGTDI	I	2: SNPU Debug interface data input
	PD1PORT05	IO	3: Domain1 GPIO 05
24	SDBGTDO	O	0: SCPU Debug interface data ouput
	DDBGTDO	O	1: DSP Debug interface data ouput
	SNDBGTDO	O	2: SNPU Debug interface data ouput
	PD1PORT06	IO	3: Domain2 GPIO 06
25	SDBGTMS	I	0: SCPU Debug interface mode select
	DDBGTMS	I	1: DSP Debug interface mode select
	SNDBGTMS	I	2: SNPU Debug interface mode select
	PCM1INBCLK	I	3: bclk of echo interface
	PD1PORT07	IO	4: Domain 1 GPIO 07
26	SDBGTCK	I	0: SCPU Debug interface clock
	DDBGTCK	I	1: DSP Debug interface clock
	SNDBGTCK	I	2: SNPU Debug interface clock
	PCM1INLRCK	I	3: lrck of echo interface
	PD1PORT08	IO	4: Domain 1 GPIO 08
27	SDBGTRST	I	0: SCPU Debug interface reset
	DDBGTRST	I	1: DSP Debug interface reset
	SNDBGTRST	I	2: SNPU Debug interface reset
	PCM1INDAT0	I	3: data of echo interface

Pin number	Signal	Type	Description
	PD1PORT09	IO	4: Domain 1 GPIO 09

5. Applications

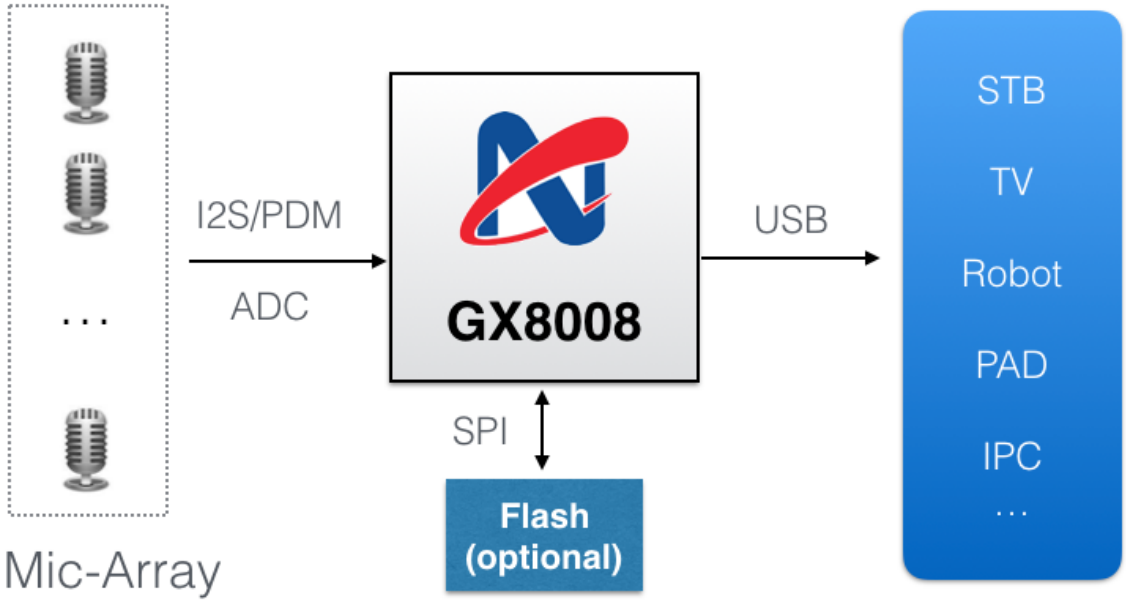


Figure 5-1 Classic GX8008 Application diagram

6. Electronic Specification

6.1. Recommended Operating Conditions

Table 6-1 Recommended Operating Conditions

Parameters	Min	Typ	Max	Units
Output High Level (VOH)	2.4	2.8	3.3	V
Output Low Level (VOL)	0	0.2	0.4	V
Input High Level (VIH)	2.0	2.8	3.6	V
Input Low Level (VIL)	-0.3	0	0.8	V
Low Level Output Current@VOL(IOL)			9.5	mA
High Level Output Current@VOH(IOH)			26.5	mA
Input Leakage Current(II)			-10	μA
Pull-up Resistor	58	86	133	kΩ
Pull-down Resistor	52	78	128	kΩ
1.1V Power Supply Voltage	1.05	1.10	1.15	V
1.1V Power Supply Current (Average)	20	200	250	mA
2.5V Power Supply Voltage	2.35	2.5	2.65	V
2.5V Power Supply Current (Average)	4.5	5	5.5	mA
3.3V Digital Power Supply Voltage	3.15	3.3	3.45	V
3.3V Digital Power Supply Current (Average)	10	15	20	mA
3.3V Analog Power Supply Voltage	3.15	3.3	3.45	V
3.3V Analog Power Supply Current (Average)	2.25	11.25	22.5	mA

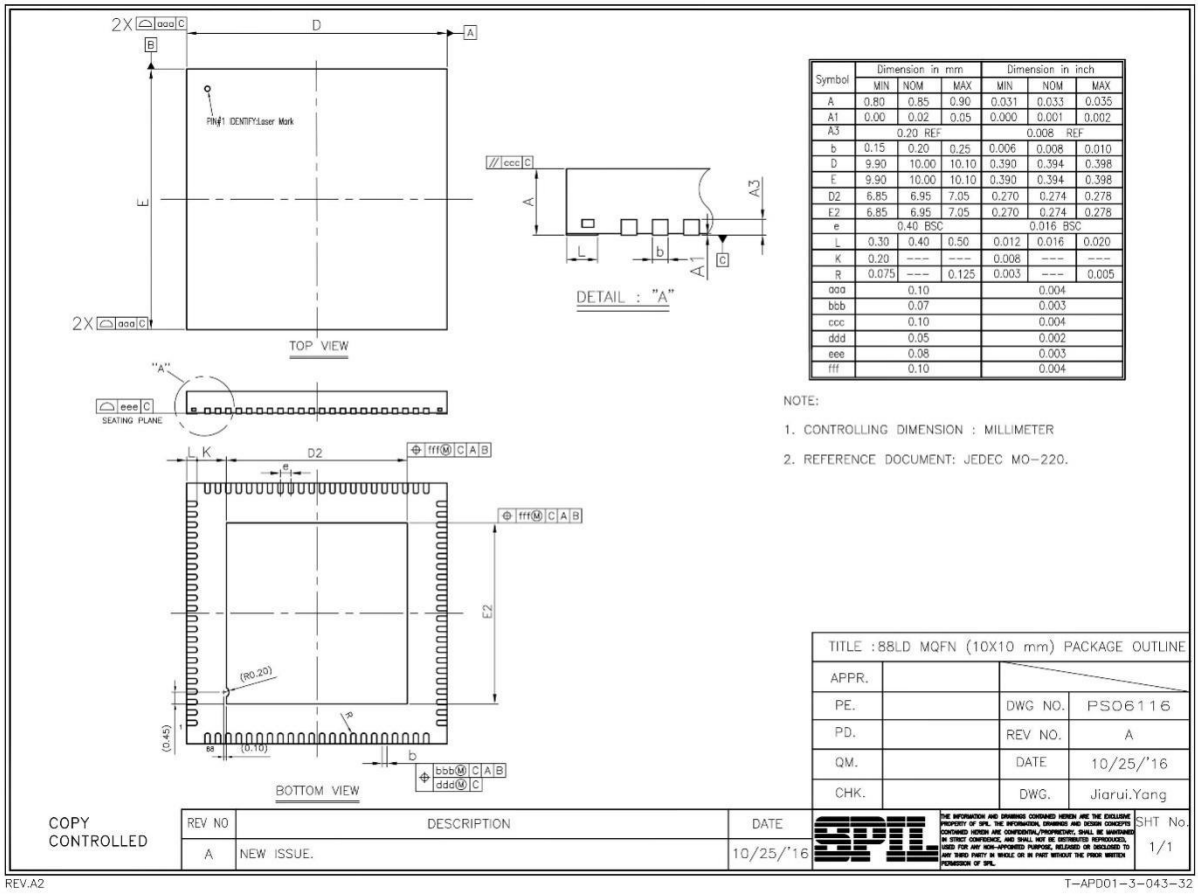
Parameters	Min	Typ	Max	Units
Leakage Current	15	24	28	mA
Operating Ambient Temperature	-20	30	95	℃
Thermal Resistance		32		℃

6.2. Absolute Maximum Ratings

Table 6-2 Absolute Maximum Ratings

Parameters	Min	Typ	Max	Units
1.1V Supply Voltages	0.99		1.21	V
2.5V Supply Voltages	2.25		2.75	V
3.3V Supply Voltages	2.8		3.6	V
Storage Temperature	-40		150	℃

7. Package Information



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D2	6.85	6.95	7.05	0.270	0.274	0.278
E2	6.85	6.95	7.05	0.270	0.274	0.278
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	0.125	0.003	---	0.005
aaa		0.10			0.004	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

Figure: 7-1 QFN88 Package Specification

8. Ordering Information

Table 8-1 GX8008 Ordering Information

Ordering Code	Description	Package
GX8008	Smart voice front-end chip	QFN88

Revision History:

Version	Time	Change Log	Author
V0.1	2017.09.01	Initial version	Robot.Ling
V1.0	2017.12.04	Fixed Pin map and description	Lin Jing
V1.1	2017.12.11	Fixed Pin map	Lin Jing
V1.2	2017.12.29	Fixed Pin map	Lin Jing
V1.3	2018.03.02	Fixed some detailed data	Lin Jing
V1.4	2018.05.25	Added pin mux	Lin Jing
V1.5	2018.06.29	Fixed some minor data	Lin Jing
V1.6	2018.11.19	Fixed electronic specification	Lin Jing
V1.7	2019.06.25	Fixed electronic specification	Lin Jing
V1.8	2019.07.01	Fixed electronic specification	Lin Jing
V1.9	2019.12.11	Fixed some detailed data	Lin Jing

Contact Information:

Hangzhou Headquarters:

Tel: +86-571-88156088
Fax: +86-571-88156083
E-mail:Marketing@nationalchip.com
Address: 5-6th Floor,Innovation Mansion East Software Park,90# Wensan Road, Hangzhou, Zhejiang Province, P.R. China ; Post Code: 310012

South China: (Shenzhen Office, in Guangdong province)

Tel: +86-755-61637134
Fax: +86-755-61637132
Address: Room 906, TCL Building, Nanshan hightech-park, Shenzhen, P.R.China

Southwest China: (Chengdu office, in Sichuan province)

Tel: +86-28-61348936
Address: Room 1603, Unit 4, Building No.7, 1st Phase of Orange Couty, China Overseas International Community, HuichuanSt., Shuxi Rd., Chengdu, P.R.China