GX8009

A Neural Processor for Smart Voice

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1. General Introduction

GX8009 is an embedded SoC chip designed for smart voice applications. Targeting at the features of AI applications, GX8009 is uniquely designed in a heterogeneous multi-core architecture, which integrates self-developed Neural Process Unit (NPU), DSP for voice processing, ARM Cortex A7 CPU, Audio decoder and other modules. It enables the product to perform deep neural network computation and process microphone array signals offline. In addition, considering the requirement of low power consumption, GX8009 is specifically assigned to support multi-level low power control, making it possible to be voice woken up even in the ultra low-power standby state. The high degree of integration of GX8009, which includes ADC, audio codec, rich peripheral interfaces as well as an embedded 64Mbyte or 128Mbyte DRAM, makes its size smaller, power consumption lower, and the entire hardware design simpler.

- The highlights of the chip includes following features:
- **NPU**:neural process unit that enables chipset to run deep learning model locally
- **sNPU**:second NPU dedicated for the model of keyword spotting.
- **CPU**:ARM CortexA7 1.0GHz with FPU and Neon DSP,with 32k/32k L1 cache,and 128KB L2 cache
- **DSP**:Tensilica HIFI4 DSP processor,speed up to 400MHz
- **Mic Array**:supports 6 analog or digital mic,both PDM and I2S
- **Audio**:supports mainstream audio format decoding and direct DAC output
- **Video**:hardware JPEG decoder and encoder
- **Security**:integrates OTP,andAES/3DES/DES engine,and support security boot and content protection.
- **Peripherals**:SPI master/Slave,SDIO master,I2C,UART,PWM, USB Slave/Master
- **Package**:SMQFN88,10x10mm

2. Chip Architecture

2.1. Block Diagram

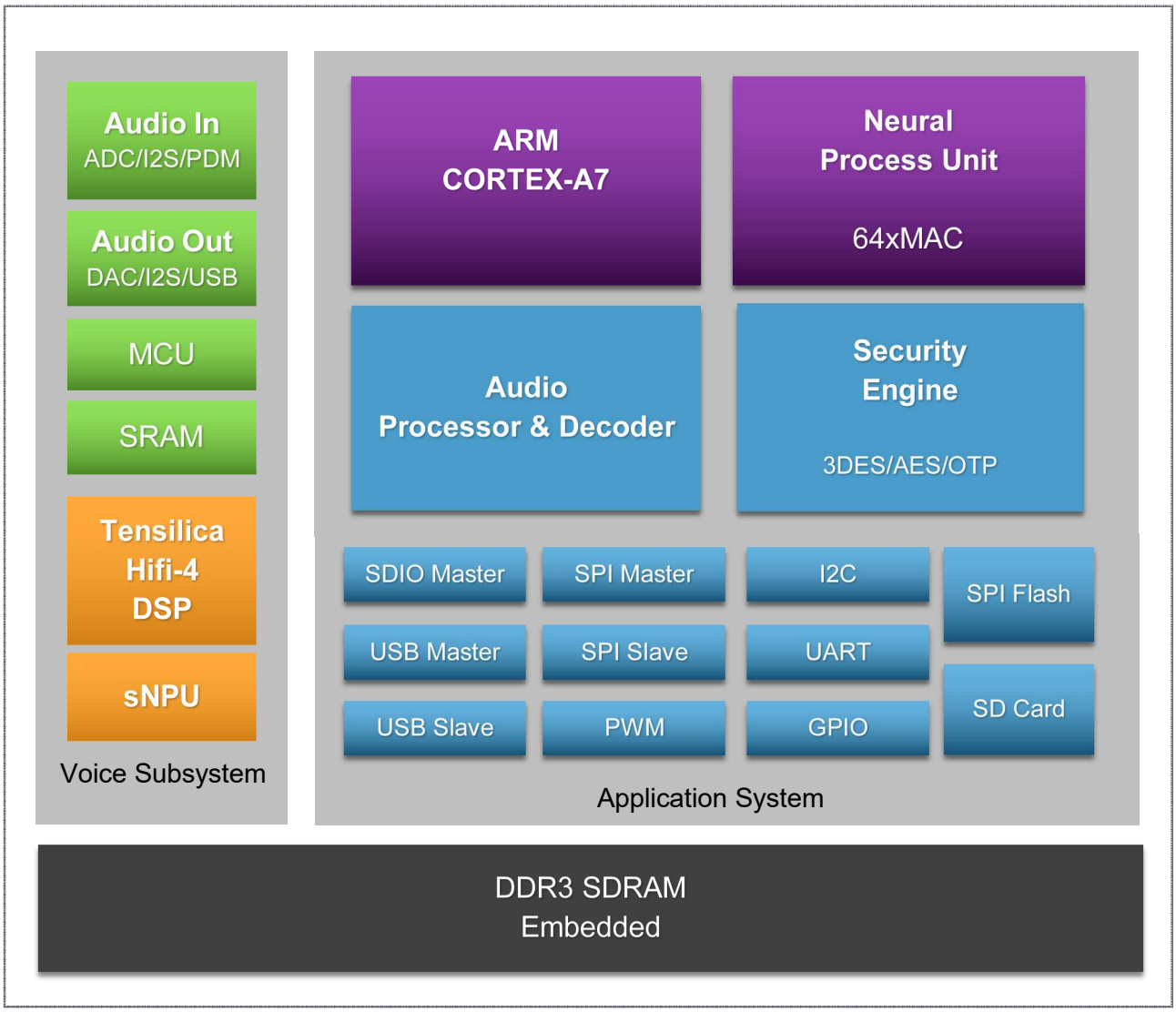


Figure 2.1 GX8009 Chip Block Diagram

The GX8009 chipset can be divided into three part: the first part is voice subsystem which process the multi-channel microphone signal and detect the wake-up keywords, the second part is application system which run the OS and the application frameworks, the last one is a SIP packaged DDR3 SDRAM which has 64Mbytes memory size.

2.2. Power Domain Specification

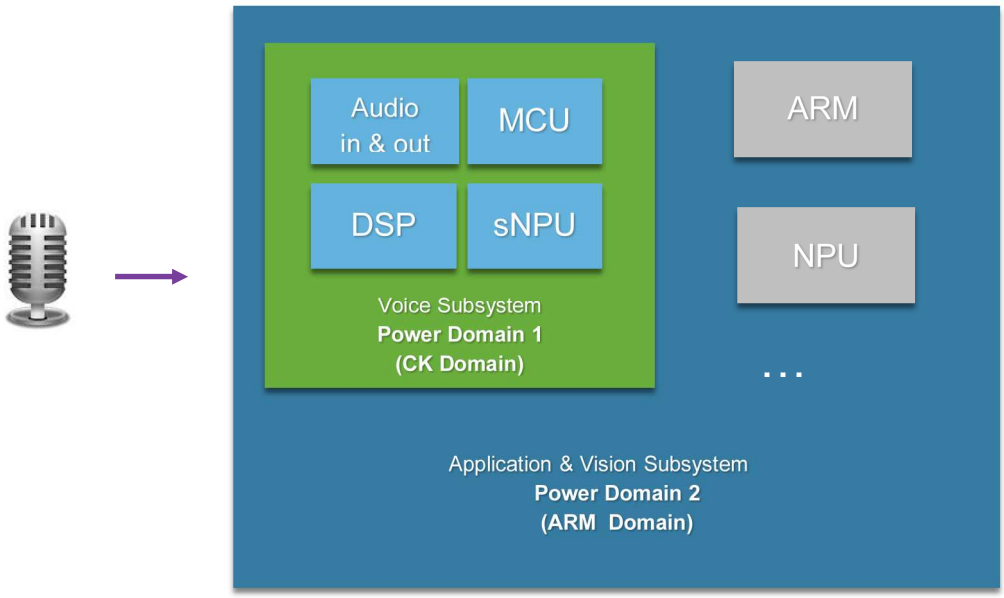


Figure 2.2 GX8009 Chip Power Domain

The GX8009 chipset internally splits into two power domain. The power domain 1 is always on and includes the modules in Voice subsystem. The modules in Application subsystem and Vision subsystem are in power domain 2. When in low-power standby mode, system can turn off the power domain 2, and power domain 1 keeps working to detect the voice command. Once the wake-up keywords were detected, the system will turn on the power domain 2.

3. Feature list

3.1. Voice Subsystem

- **DSP:**
    - Cadence Tensilica HIFI4 voice and audio DSP, frequency up to 400MHz
    - Quad 32-bit MAC, eight 16-bit MAC, up to 3.2GOPS.
    - 32KB Instruction Cache, 32KB Data Cache
    - 32KB DTCM, 32KB PTCM
    - Support JTAG
- **sNPU:**
    - Neural process unit dedicated for keywords spotting
    - 32 MAC, up to 12GOPS
    - support DNN/CNN/LSTM and other classic models.
- **MCU:**
    - 32bit RISC MCU, frequency up to 150MHz
    - System booting and low power standby control
    - Coordinate the work flow of DSP, sNPU and the main CPU
- **Digital Mic Input:**
    - Support maximum 6 channel digital mic signal input
    - Support I2S and PDM
- **Analog Mic Input:**
    - Integrate 16-bit 6 channel Sigma-Delta ADC
    - Sample rate: 8KHz, 16KHz, 48KHz
    - Integrate PGA amplifier for each channel, 2dB per step
    - SNR: 85dB
- **Audio Output:**
    - Dual channel 16-bit DAC with up to 95dB SNR

- SPDIF and I2S output
- USB 2.0 full speed slave mode, support USB audio class

3.2. Application System

- **NPU (Neural Process Unit)**
  - Neural Process Unit, enable the chipset to run neural models locally
  - 64 MAC array, up to 38GOPS
  - Support float32 and float16 data format
  - Support DNN/CNN/LSTM and other classic deep learning models.
  - Support activation function such as Sigmoid, Tanh, Relu, Soft plus
  - Support neural network weights compression
  - Tensorflow compatible
- **CPU**
  - ARM Cortex A7 up to 1.0GHz
  - 32KB L1 instruction cache, 32KB L1 data cache, and 128KB L2 cache
  - Integrate FPU and Neon DSP
  - Support dynamic frequency adjustment
- **Memory**
  - Support SPI Nor and Nand Flash, maximum size up to 256MB
  - Support SD card
  - Embbed 512Mb DDR3 up to 533MHz
- **Audio Processor and Decoder:**
  - MPEG1 I/II, Layer I/II, MP3 decoding
  - MPEG-4 AAC and AAC plus (HE-AAC v1 and v2) decoding
  - 3 channel audio mixing
  - Audio sample rate conversion

- **Communication System**
  - I2Cx2
  - USB 2.0 high speed host interface for external devices
  - USB 2.0 high speed slave interface for UAC、HID and debug port
  - General purpose DMA
  - General purpose SDIO/SPI Master
  - SPI slave
  - Timerx4
  - SD card controllerx2
  - UARTx3
  - PWM controller
  - GPIO
- **Security Engine**
  - Integrate OTP
  - Unique ID per chip
  - Integrate AES/DES/3DES engine
  - Support security boot
  - Support content protection for NPU models

4. Pin Map

4.1. Pin Map

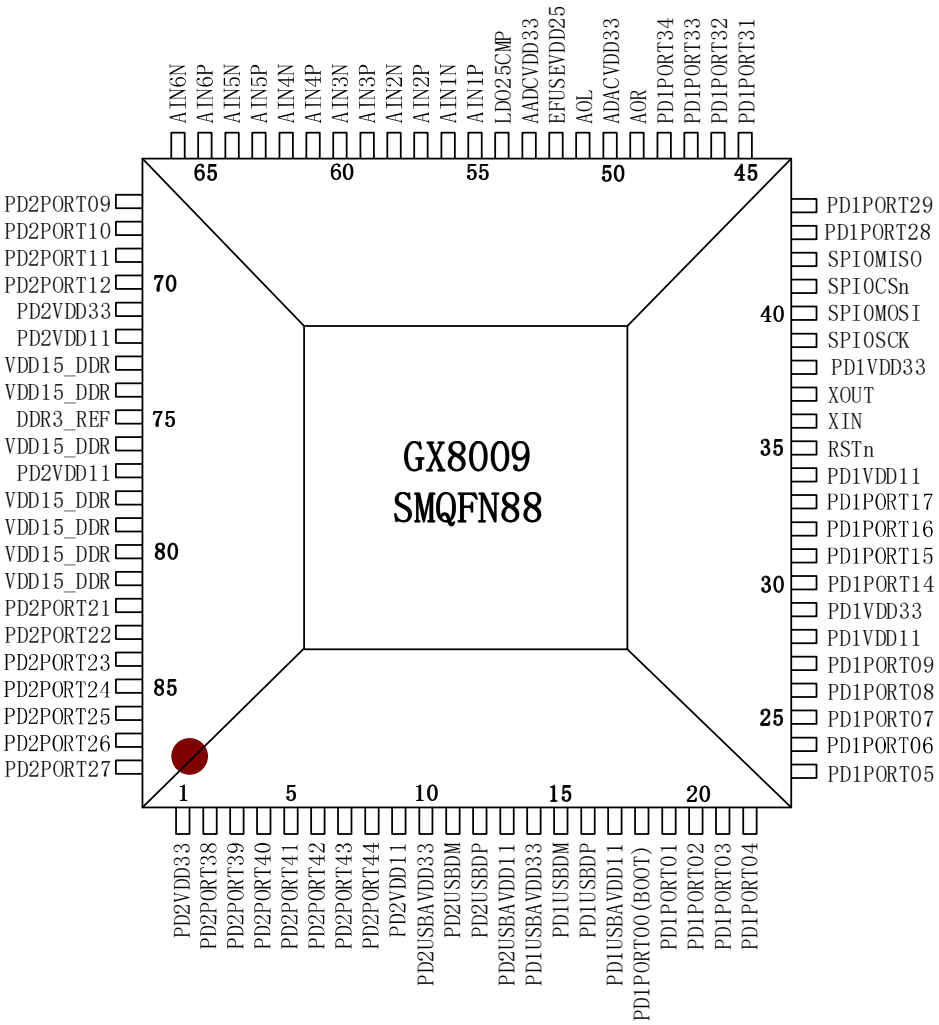


Figure 4.1 GX8009 Pin Configuration

4.2. Acronyms

DP => Digital Power
AP => Analog Power
AI => Analog Input
I => Digital Input
IO => Digital Bi-directional

DG => Digital Ground
AG => Analog Ground
AO => Analog Output
O => Digital Output
AB => Analog Bi-directional

4.3. Pin Mux

Table 4-1 Pin Mux

Domain	PORT_NAME	PULL	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3	FUNCTION4	FUNCTION5
CK Domain	PD1PORT00	UP	GPIO0					
CK Domain	PD1PORT01		POWER_DOWN	GPIO1				
CK Domain	PD1PORT02	UP	UART0_RX	GPIO2				
CK Domain	PD1PORT03		UART0_TX	GPIO3				
CK Domain	PD1PORT04		OTP_AVDD_EN	GPIO4				
CK Domain	PD1PORT05	UP	SDBGTDI	DDBGTDI	SNDBGTDI	GPIO5		
CK Domain	PD1PORT06		SDBGTDO	DDBGTDO	SNDBGTDO	GPIO6		
CK Domain	PD1PORT07	UP	SDBGTMS	DDBGTMS	SNDBGTMS	PCM1INBCLK	GPIO7	
CK Domain	PD1PORT08	UP	SDBGTCK	DDBGTCK	SNDBGTCK	PCM1INLRCK	GPIO8	
CK Domain	PD1PORT09	UP	SDBGTRST	DDBGTRST	SNBGTRST	PCM1INDAT0	GPIO9	
CK Domain	PD1PORT14		PCMOUTMCLK	DUART_TX	GPIO14			
CK Domain	PD1PORT15		PCMOUTDAT0	SPDIF	GPIO15			
CK Domain	PD1PORT16		PCMOUTLRCK	GPIO16				
CK Domain	PD1PORT17		PCMOUTBCLK	GPIO17				
CK Domain	PD1PORT28	UP	SDA1	GPIO28				
CK Domain	PD1PORT29	UP	SCL1	GPIO29				
CK Domain	PD1PORT31	UP	PCM0INDAT0	PDMDAT2	GPIO31			
CK Domain	PD1PORT32		PCM0INMCLK	PDMDAT1	GPIO32			
CK Domain	PD1PORT33	UP	PCM0INLRCK	PDMDAT0	PCM0OUTLRCK	GPIO33		
CK Domain	PD1PORT34	UP	PCM0INBCLK	PDMCLK	PCM0OUTBCLK	GPIO34		
CK Domain	SPI0SCK		SPI0SCK					
CK Domain	SPI0MOSI	UP	SPI0MOSI					
CK Domain	SPI0CSn	UP	SPI0CSn					
CK Domain	SPI0MISO	UP	SPI0MISO					
ARM Domain	PD2PORT09	UP		SDA2	SPI1SCK	GPIO9		

Domain	PORT_NAME	PULL	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3	FUNCTION4	FUNCTION5
ARM Domain	PD2PORT10	UP		SCL2	SPI1MOSI	GPIO10		
ARM Domain	PD2PORT11	UP		UART2_RX	SPI1CSn	GPIO11		
ARM Domain	PD2PORT12	UP		UART2_TX	SPI1MISO	NUART_TX	AUART_TX	GPIO12
ARM Domain	PD2PORT21	UP	UART3_RX	SD1CDn	SDA3	GPIO21		
ARM Domain	PD2PORT22		UART3_TX	SD1DAT1	SCL3	GPIO22		
ARM Domain	PD2PORT23	UP	DBGTDI	SD1DAT0	SPI2SCK	GPIO23		
ARM Domain	PD2PORT24		DBGTDO	SD1CLK	SPI2MOSI	GPIO24		
ARM Domain	PD2PORT25	UP	DBGTMS	SD1CMD	SPI2CSn	GPIO25		
ARM Domain	PD2PORT26	UP	DBGTCK	SD1DAT3	SPI2MISO	GPIO26		
ARM Domain	PD2PORT27	UP	DBGTRST	SD1DAT2	GPIO27			
ARM Domain	PD2PORT38	UP	SD0CDn	GPIO38				
ARM Domain	PD2PORT39	UP	SD0DAT1	GPIO39				
ARM Domain	PD2PORT40	UP	SD0DAT0	GPIO40				
ARM Domain	PD2PORT41		SD0CLK	GPIO41				
ARM Domain	PD2PORT42	UP	SD0CMD	GPIO42				
ARM Domain	PD2PORT43	UP	SD0DAT3	GPIO43				
ARM Domain	PD2PORT44	UP	SD0DAT2	GPIO44				

4.4. CK Domain Power and Ground Pins

Table 4-2 Power and Ground Pins

Pin Number	Signal	Type	Description
29,38	PD1VDD33	DP	3.3V digital power for IO
28,34	PD1VDD11	DP	1.1V digital power for core
50	ADACVDD33	AP	Power (3.3V) for Audio DAC
52	EFUSE2.5	AP	Power (2.5V) for EFUSE

Pin Number	Signal	Type	Description
53	ADCVDD33	AP	Power (3.3V) for Audio ADC
54	LDO25CMP	AP	Power (2.5V) for ADC power compensate
14	PD1USBVDD33	AP	Power (3.3V) for USB Slave
17	PD1USBVDD11	AP	Power (1.1V) for USB Slave

4.5. CK Domain System Operation Pins

Table 4- 3 System Operation Pins

Pin Number	Signal	Type	Description
36	XIN	I	Clock input or crystal input
37	XOUT	O	Output for crystal connection
35	RSTn	I	System reset, active low

4.6. CK Domain ADC Interface Signals

Table 4- 4 ADC Interface Signal Pins

Pin Number	Signal	Type	Description
55	ADCIN1_P	AI	Differential Voltage Inputs, Channel 1
56	ADCIN1_N	AI	Differential Voltage Inputs, Channel 1
57	ADCIN2_P	AI	Differential Voltage Inputs, Channel 2
58	ADCIN2_N	AI	Differential Voltage Inputs, Channel 2
59	ADCIN3_P	AI	Differential Voltage Inputs, Channel 3

Pin Number	Signal	Type	Description
60	ADCIN3_N	AI	Differential Voltage Inputs, Channel 3
61	ADCIN4_P	AI	Differential Voltage Inputs, Channel 4
62	ADCIN4_N	AI	Differential Voltage Inputs, Channel 4
63	ADCIN5_P	AI	Differential Voltage Inputs, Channel 5
64	ADCIN5_N	AI	Differential Voltage Inputs, Channel 5
65	ADCIN6_P	AI	Differential Voltage Inputs, Channel 6
66	ADCIN6_N	AI	Differential Voltage Inputs, Channel 6

4.7. CK Domain SPI Flash Signals

Table 4-5 Flash Signals

Pin Number	Signal	Type	Description
39	SPISCK	O	SCK of SPI interface
40	SPIMOSI	IO	MOSI of SPI interface
41	SPICSn	O	CS of SPI interface
42	SPIMISO	IO	MISO of SPI interface

4.8. CK Domain Audio Play Interface Signals

Table 4- 6 Audio Paly Interface Signals

Pin Number	Signal	Type	Description
49	AOR	AO	Audio DAC right channel output

Pin Number	Signal	Type	Description
51	AOL	AO	Audio DAC left channel output
30	PCMOUTMCLK	O	0: mclk of audio out i2s interface
	DUARTTX	O	1: DSP UART data transmit
	SNUARTTX	O	2: SNPU UART data transmit
	PD1PORT14	IO	3: Domain1 GPIO 14
31	PCMOUTDAT0	O	0: data0 of audio out I2S interface
	SPDIF	O	1: Sony/Philips Digital Interface Format
	PD1PORT15	IO	2: Domain1 GPIO 15
32	PCMOUTLRCK	O	0: lrclk of audio in0 i2s interface
	PD1PORT16	IO	1: Domain1 GPIO 16
33	PCMOUTBCLK	O	0: bclk of audio out i2s interface
	PD1PORT17	IO	1: Domain1 GPIO 17

4.9. CK Domain Communication Interface Signals

Table 4- 7 Communication Interface Signals

Pin Number	Signal	Type	Description
43	SDA1	IO	0: Data of I2C 1
	PD1PORT28	IO	1: Domain1 GPIO 28
44	SCL1	IO	0:Clock of I2C 1
	PD1PORT29	IO	1: Domain1 GPIO 29

Pin Number	Signal	Type	Description
22	PD1PORT04	IO	0: Domain1 GPIO 04
21	UART0TX	O	0: UART0 data transmit
	PD1PORT03	IO	1: Domain1 GPIO 03
20	UART0RX	O	0: UART0 data receive
	PD1PORT02	IO	1: Domain1 GPIO 02
19	POWER_DOWN	O	0: CK Domain Power_down Controller
	PD1PORT01	IO	1: Domain1 GPIO 01
18	BOOT	I	0: Boot key
	PD1PORT00	IO	1: Domain1 GPIO 00

4.10.CK Domain Audio In Interface Signals

Table 4- 8 Audio In Interface Signals

Pin Number	Signal	Type	Description
45	PCM0INDAT0	I	0: data0 of audio in0 i2s interface
	PDMDAT2	I	1: data2 of audio in pdm interface
	PD1PORT31	IO	2: Domain1 GPIO 31
46	PCM0INMCLK	I	0: mclk of audio in0 i2s interface
	PDMDAT1	I	1: data1 of audio in pdm interface
	PD1PORT32	IO	2: Domain1 GPIO 32
47	PCM0INLRCK	I	0: lrck of audio in0 i2s interface

Pin Number	Signal	Type	Description
	PDMDAT0	I	1: data0 of audio in pdm interface
	PCM0OUTLRCK	O	2: lrck of audio out i2s interface from core
	PD1PORT33	IO	3: Domain1 GPIO 33
48	PCM0INBCLK	I	0: bclk of audio in0 i2s interface
	PDMCLK	O	1: clk of audio in pdm interface
	PCM0OUTBCLK	O	2: bclk of audio out i2s interface from core
	PD1PORT34	IO	3: Domain1 GPIO 34

4.11. CK Domain USB Slave Interface Signals

Table 4- 9 USB Slave Interface Signals

Pin number	Signal	Type	Description
16	PD1USBDP	AB	USB Slave Data pin Data+
15	PD1USBDM	AB	USB Slave Data pin Data-

4.12. CK Domain JTAG Interface Signals

Table 4- 10 JTAG Interface Signals

Pin Number	Signal	Type	Description
23	SDBGTDI	I	0: SCPU Debug interface data input
	DDBGTDI	I	1: DSP Debug interface data input
	SNDBGTDI	O	2: SNPU Debug interface data input

Pin Number	Signal	Type	Description
	PD1PORT05	IO	3: Domain1 GPIO 05
24	SDBGTDO	O	0: SCPU Debug interface data ouput
	DDBGTDO	O	1: DSP Debug interface data ouput
	SNDBGTDO	O	2: SNPU Debug interface data ouput
	PD1PORT06	IO	3: Domain1 GPIO 06
25	SDBGTMS	I	0: SCPU Debug interface mode select
	DDBGTMS	I	1: DSP Debug interface mode select
	SNDBGTMS	I	2: SNPU Debug interface mode select
	PCM1INBCLK	I	3: bclk of echo interface
	PD1PORT07	IO	4: Domain 1 GPIO 07
26	SDBGTCK	I	0: SCPU Debug interface clock
	DDBGTCK	I	1: DSP Debug interface clock
	SNDBGTCK	I	2: SNPU Debug interface clock
	PCM1INLRCK	I	3: lrck of echo interface
	PD1PORT08	IO	4: Domain 1 GPIO 08
27	SDBGTRST	I	0: SCPU Debug interface reset
	DDBGTRST	I	1: DSP Debug interface reset
	SNDBGTRST	I	2: SNPU Debug interface reset
	PCM1INDAT0	I	3: data of echo interface
	PD1PORT09	IO	4: Domain 1 GPIO 09

4.13.ARM Domain Power and Ground Pins

Table 4- 11 Power and Ground Pins

Pin Number	Signal	Type	Description
1,71	PD2VDD33	DP	3.3V digital power for IO
9，72，77	PD2VDD11	DP	1.1V digital power for core
73,74,76,78, 79,80,81	DDRVDD	AP	Power (1.5V) for DDR3
10	PD2USBVDD33	AP	Power (3.3V) for USB Host
13	PD2USBVDD11	AP	Power (1.1V) for USB Host

4.14.ARM Domain Communication Interface Signals

Table 4-12 Communication Interface Signals

Pin Number	Signal	Type	Description
67	SDA2	IO	0:Data of I2C 2
	SPI1SCK	O	1:SCK of SPI interface 1
	PD1PORT09	IO	2: Domain 2 GPIO 09
68	SCL2	IO	0: Clock of I2C 2
	SPI1MOSI	IO	1: MOSI of SPI interface 1
	PD2PORT10	IO	2: Domain 2 GPIO 10
69	UART2RX	I	0: UART2 data receive
	SPI1MOSI	IO	1: MOSI of SPI interface 1
	PD2PORT11	IO	2: Domain 2 GPIO 11

Pin Number	Signal	Type	Description
70	UART2TX	I	0: UART2 data receive
	SPI1CSn	IO	1: CSn of SPI interface 1
	NUARTTX	IO	2: NPU UART data transmit
	AUARTTX	IO	3: Audio OR UART data transmit
	PD2PORT12	IO	4: Domain 2 GPIO 12

4.15.ARM Domain USB Interface Signals

Table 4-13 USB Interface Signals

Pin Number	Signal	Type	Description
12	PD2USBDP	IO	USB Host Data pin Data+
11	PD2USBDM	IO	USB Host Data pin Data-

4.16.ARM Domain SPI Interface Signals

Table 4-14 SPI Interface Signals

Pin Number	Signal	Type	Description
82	UART3RX	I	0: UART3 data receive
	SD1CDn	I	1: Card Detect of SDIO Interface 1
	SDA3	IO	2:Data of I2C 3
	PD2PORT21	IO	3: Domain 2 GPIO 21
83	UART3TX	O	0: UART3 data transmit

Pin Number	Signal	Type	Description
	SD1DAT1	I	1: Data Line 1 of SDIO Interface 1
	SCL3	IO	2: Clock of I2C 3
	PD2PORT22	IO	3: Domain 2 GPIO 21
84	DBGTDI	I	0: ARM Debug interface data input
	SD1DAT0	IO	1: Data Line 0 of SDIO Interface 1
	SPI2SCK	IO	2: SCK of SPI interface 2
	PD2PORT23	IO	3: Domain 2 GPIO 23
85	DBGTD0	O	0: ARM Debug interface data output
	SD1CLK	O	1: clk of SDIO Interface 1
	SPI2MOSI	IO	2: MOSI of SPI interface 2
	PD2PORT24	IO	3: Domain 2 GPIO 24
86	DBGTMS	I	0: ARM Debug interface mode select
	SD1CMD	IO	1: Command of SDIO Interface 1
	SPI2CSn	IO	2: CSn of SPI interface 2
	PD2PORT25	IO	3: Domain 2 GPIO 25
87	DBGTCK	I	0: ARM Debug interface clock
	SD1DAT3	IO	1: data line 3 SDIO Interface 1
	SPI2MISO	IO	2: MISO of SPI interface 2
	PD2PORT26	IO	3: Domain 2 GPIO 26
88	DBGTRST	I	0: ARM Debug interface clock

Pin Number	Signal	Type	Description
	SD1DAT2	IO	1: data line 2 of SDIO Interface 1
	PD2PORT27	IO	3: Domain 2 GPIO 27

4.17.ARM Domain SDIO Interface Signals

Table 4-15 SDIO Interface Signals

Pin Number	Signal	Type	Description
2	SD0CDn	I	0: Card Detect of SDIO Interface 0
	PD2PORT38	IO	1: Domain 2 GPIO 38
3	SD0DAT1	IO	0: Data Line 1 of SDIO Interface 0
	PD2PORT39	IO	1: Domain 2 GPIO 39
4	SD0DAT0	IO	0: Data Line 0 of SDIO Interface 0
	PD2PORT40	IO	1: Domain 2 GPIO 40
5	SD0CLK	IO	0: Clock of SDIO Interface 0
	PD2PORT41	IO	1: Domain 2 GPIO 41
6	SD0CMD	IO	0: Command of SDIO Interface 0
	PD2PORT42	IO	1: Domain 2 GPIO 42
7	SD0DAT3	IO	0: Data Line 3 of SDIO Interface 0
	PD2PORT43	IO	1: Domain 2 GPIO 43
8	SD0DAT2	IO	0: Data Line 2 of SDIO Interface 0
	PD2PORT44	IO	1: Domain 2 GPIO 44

5. Applications

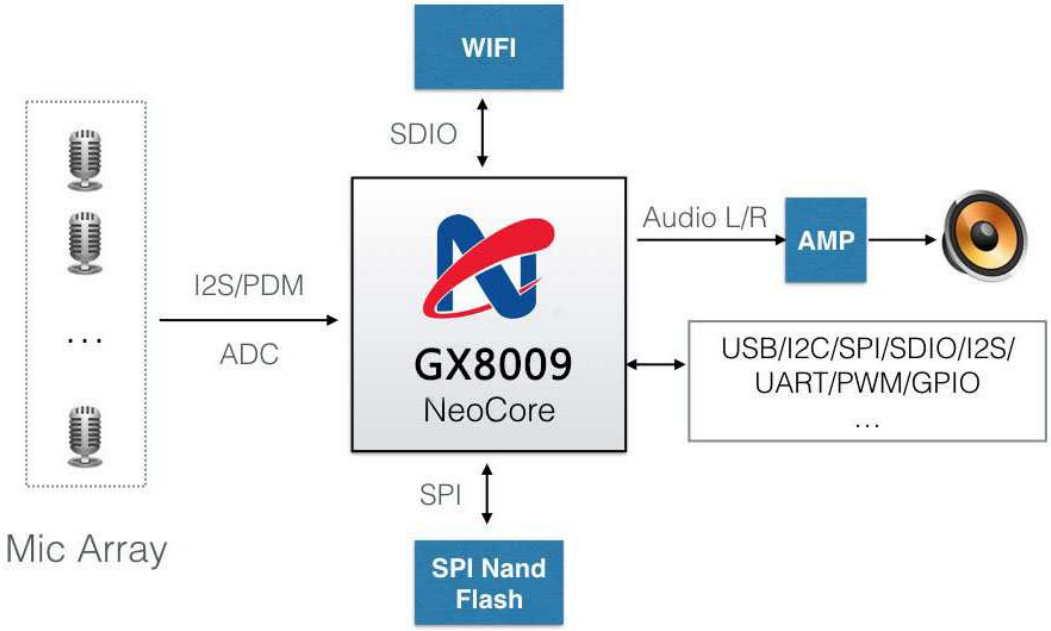


Figure 5.1 Classic GX8009 Application Diagram

6. Electronic Specification

6.1. Recommended operating conditions

Table 6- 1 Recommended operating conditions

Parameters	Min	Typ	Max	Units
Output High Level (VOH)	2.4	2.8	3.3	V
Output Low Level (VOL)	0	0.2	0.4	V
Input High Level (VIH)	2.0	2.8	3.6	V
Input Low Level (VIL)	-0.3	0	0.8	V
Low Level Output Current@VOL(IOL)			9.5	mA
High Level Output Current@VOH(IOH)			26.5	mA
Input Leakage Current(II)			-10	μA
Pull-up Resistor	58	86	133	kΩ
Pull-down Resistor	52	78	128	kΩ
Storage Temperature	-40		150	℃
Operating Ambient Temperature	-20	30	95	℃
Thermal Resistance		29		℃

6.2. Electronic Characteristics of CK Domain

Table 6- 2 Electronic characteristics of CK Domain

Parameters	Min	Typ	Max	Units
1.1V Power Supply Voltage	1.05	1.10	1.21	V
1.1V Power Supply Current (Average)	20	200	250	mA

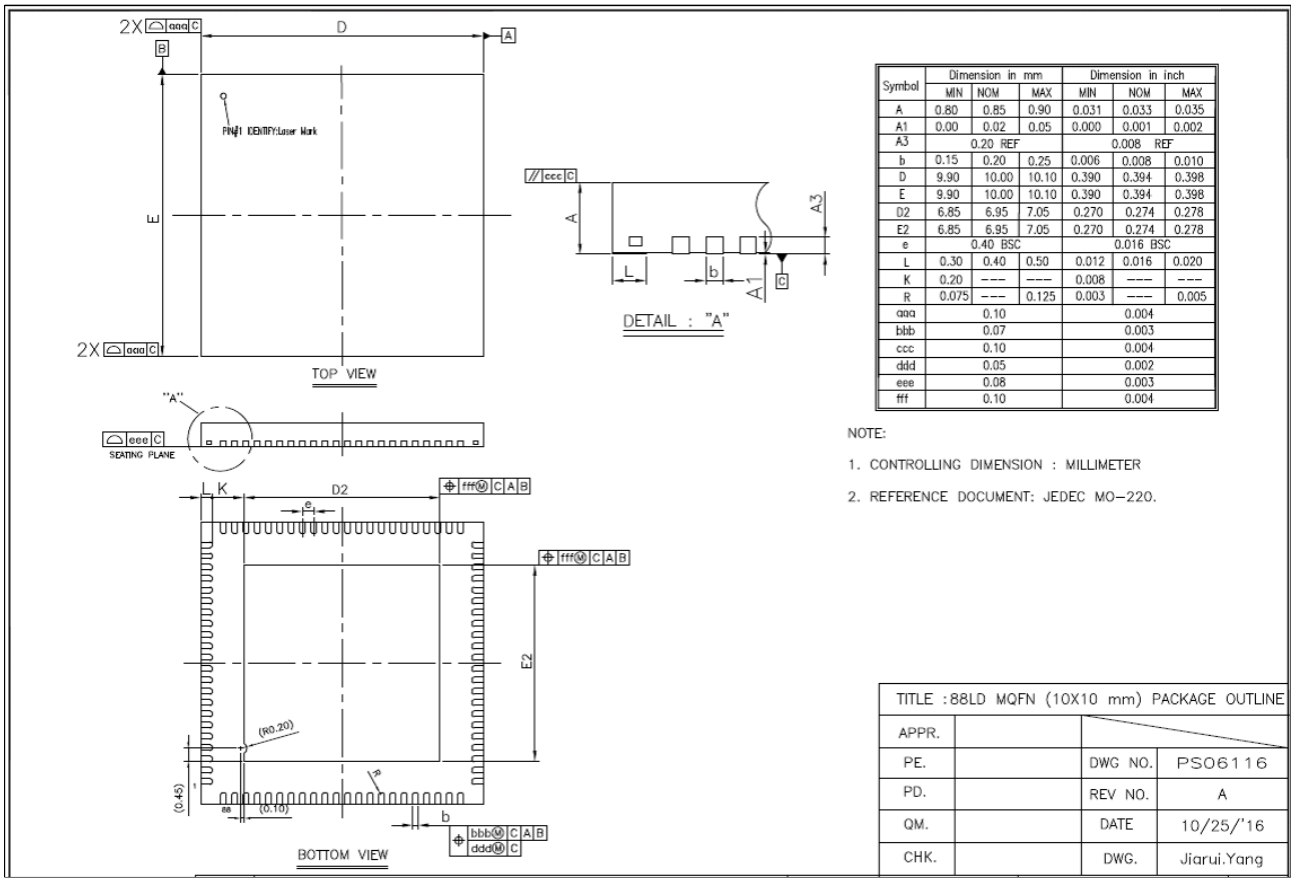
Parameters	Min	Typ	Max	Units
2.5V Power Supply Voltage	2.25	2.5	2.75	V
2.5V Power Supply Current (Average)	4.5	5	5.5	mA
3.3V Digital Power Supply Voltage	2.8	3.3	3.6	V
3.3V Digital Power Supply Current (Average)	10	15	20	mA
3.3V Analog Power Supply Voltage	2.8	3.3	3.6	V
3.3V Analog Power Supply Current (Average)	2.25	11.25	22.5	mA
Leakage Current	15	24	28	mA

6.3. Electronic Characteristics of ARM Domain

Table 6- 3 Electronic Characteristics of ARM Domain

Parameters	Min	Typ	Max	Units
1.1V Power Supply Voltage	1.05	1.10	1.21	V
1.1V Power Supply Current (Average)	55	380	500	mA
1.5V Power Supply Voltage	1.35	1.5	1.65	V
1.5V Power Supply Current (Average)	10	80	130	mA
3.3V Digital Power Supply Voltage	2.8	3.3	3.6	V
3.3V Digital Power Supply Current (Average)	10	15	20	mA
Leakage Current	32	40	50	mA

7. Package Information



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D2	6.85	6.95	7.05	0.270	0.274	0.278
E2	6.85	6.95	7.05	0.270	0.274	0.278
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	0.125	0.003	---	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

Figure: 7.1 SMQFN88 Package parameters

8. Ordering Information

Table 8- 1 GX8009 Ordering Information

Ordering Code	CPU Frequency	Embedded DDR	Package
GX8009A	1.0GHz	64M bytes	SMQFN88
GX8009B	1.0GHz	128M bytes	SMQFN88

Revision History:

Version	Time	Change Log	Author
V1.0	2018.05.20	Initial version.	Chen Shu
V1.1	2018.06.29	Fixed some minor mistake.	Lin Jing
V1.2	2018.10.10	Fixed pin numbers.	Lin Jing
V1.3	2018.11.19	Fixed electronic specification.	Lin Jing
V1.4	2019.02.27	Added new ordering code.	Lin Jing
V1.5	2019.05.24	Fixed Feature Data.	Lin Jing
V1.6	2019.09.24	Fixed electronic specification.	Lin Jing
V1.7	2019.12.11	Fixed pin infomation.	Lin Jing
V1.8	2020.08.26	Fixed CPU frequency.	Lin Jing

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