GX8301
Low-power BLE SoC
Datasheet

Revision History:

Version	Time	Change Log	Author
V0.1	2022.8.15	Initial	Robot.Ling
V0.2	2022.9.14	Modify Pin map and Multi-function IO Signals.	Robot.Ling
V0.3	2023.2.27	Fixed some minor mistakes.Update PMU block diagram.	Robot.Ling
V0.4	2023.5.3	Add more package types and modify some feature changes.	Robot.Ling
V0.5	2023.6.28	Modify Pin map and pin description. Update package and chip mark description. Add descripition about bluetooth. Modify QFN32 package parameters.	Liqr
V0.6	2023.7.25	Update applications.Fixed some minor mistakes.	Liqr
V0.7	2023.10.19	Update pin map and pin description Update IO function list and bt features.	Liqr
V0.8	2024.1.9	Add power consumption,add RF performance,add ADC and Lodac characteristics.Update ON/OFF IO description.	Liqr
V0.9	2024.1.16	Update RF performance data,Update SIP flash frequency.	Liqr
V1.0	2024.4.19	Fixed some minor mistakes.	Liqr
V1.1	2024.10.22	Update por&bor description.Delete lpc description.Update sleep mode power consumption.	Liqr

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1. Key Features

GX8301 is a low-power SoC with Bluetooth LE and high performance CPU system. The chip integrates BLE radio & baseband, CPU, audio system, RAM, Flash and rich peripherals. The chip is powerful and flexible to various BLE and audio applications.

Bluetooth

- Bluetooth Low Energy V5.4 qualified
- Support 1Mbps, 2Mbps, and 125K/500K coded PHY, support LE Audio
- Support 2.4G proprietary mode
- RX sensitivity: -96dBm
- TX power: 7dBm

CPU

- 32bit RISC-V CPU with I/D Cache, DSP and FPU. Core mark up to 3.6
- Frequency up to 96 MHz
- Support audio decode and encode

Memory

- Built-in 128KB SRAM
- Support external PSRAM
- SIP Nor Flash, size 512KB

Audio

- 16bit Sigma-Delta Audio ADC, with SNR 90dB. Support PGA from 0~32dB
- 2 channel PDM microphone interface
- I2S input and output, support master mode and slave mode. Support TDM mode
- Sample rate support 16k/32k/48k/96k

System

- Use 32MHz crystal
- Internal 32kHz and 32Mhz OSC
- Power on reset

Peripherals

- Key scan controller, matrix key scan and determinant key scan
- 2 QSPI master or slave
- SDIO 2.0 master
- 2 UARTs, up to 3Mbps
- 3 I2C controller, support 1Mbps
- USB 2.0 full speed device
- 12bit 8 channel SAR-ADC
- PWM controller
- Infra-red receiver and transmitter
- 3 channel quad decoder
- 8 Timers, 1 watch dog timer and 1 RTC
- General purples DMA

Power management

- Wide Input voltage range: 1.8~5.5v
- Build in DCDC and LDO
- Typical power consumption:
  - Ship Mode: 250nA@3V
  - Deep Sleep without RC and 80KB-SRAM retension, all GPIO or M scan mode wake-up:850nA@3V
  - Deep Sleep with RC and 80KB-SRAM retension: 1.55uA@3V
  - BLE sniff @500ms: 30uA

Package

- QFN32 4x4, pitch 0.4
- QFN52 6x6, pitch 0.4

2. Chip architecture

2.1. Block diagram

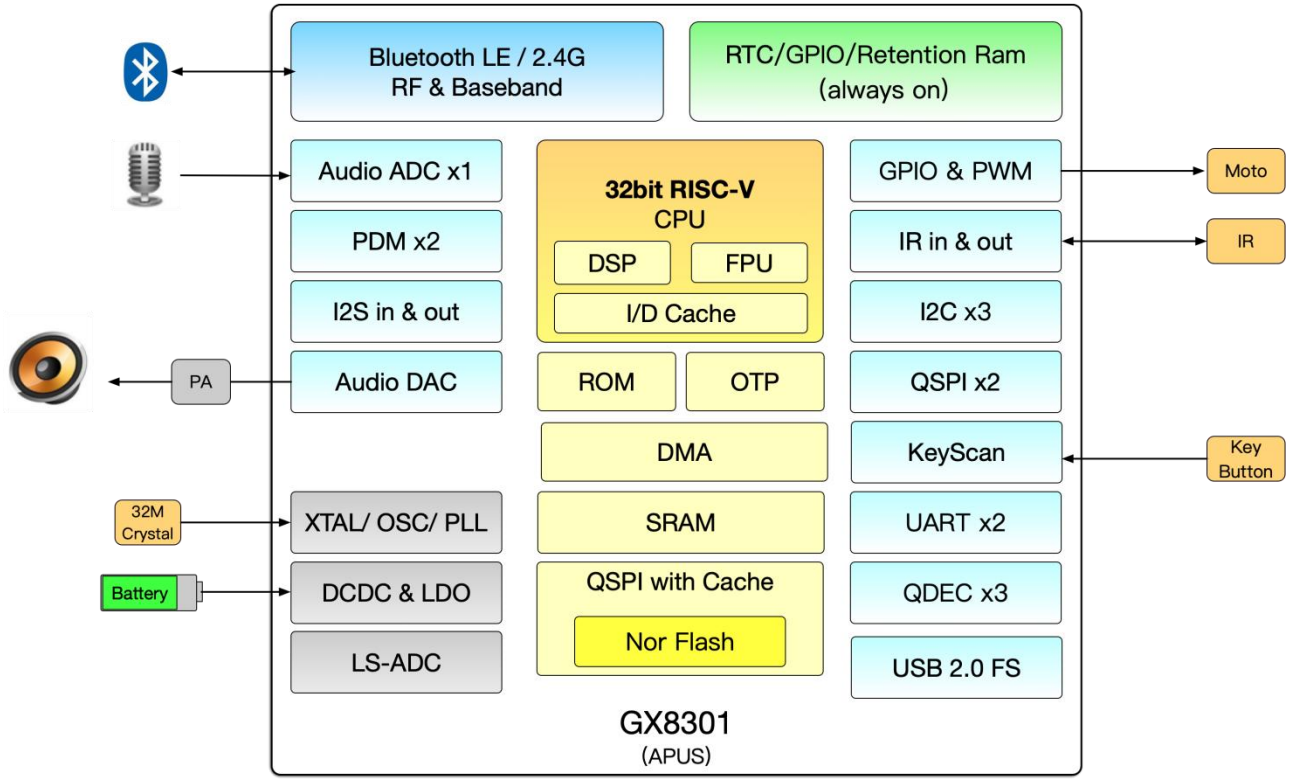


Figure 2.1 GX8301 Chip block diagram

3. Pin map

3.1. Acronyms

DP => Digital Power

DG => Digital Ground

AP => Analog Power

AG => Analog Ground

AI => Analog Input

AO => Analog Output

I => Digital Input

O => Digital Output

IO => Digital Bi-directional

3.2. GX8301A pin map

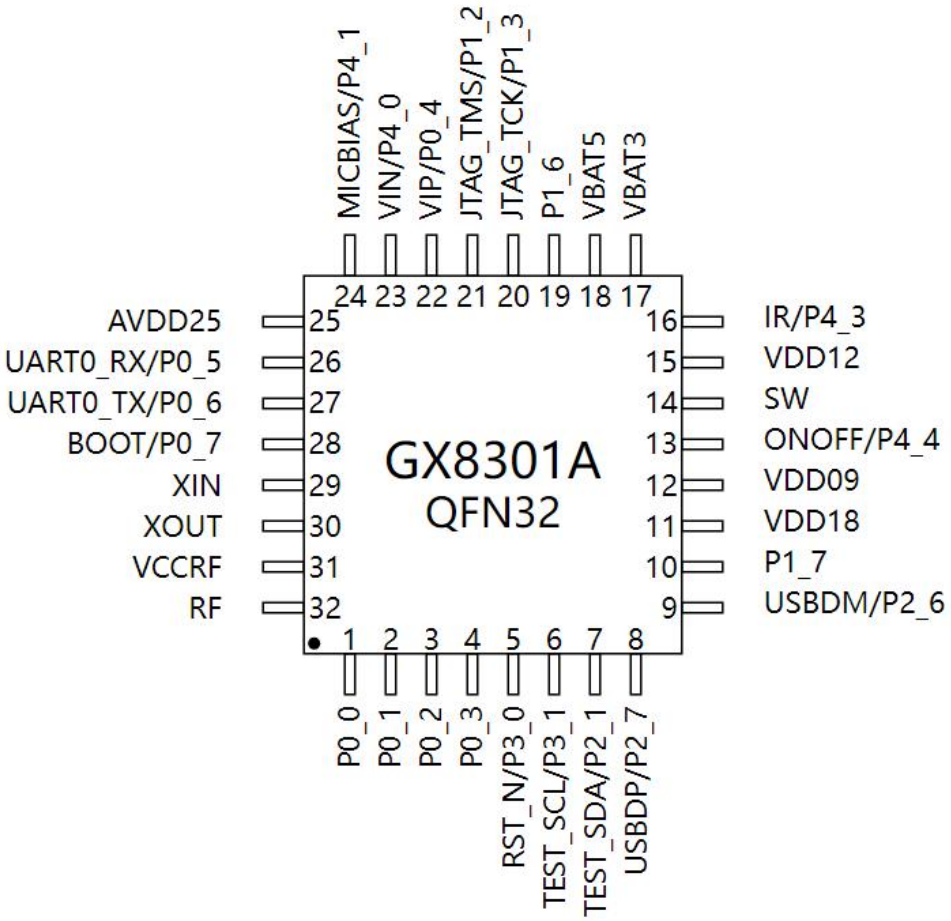


Figure 3.1 GX8301A Pin map

3.3. GX8301A pin description

Pin Number	Pin Name	Type	Domain	Description
1	P0_0	IO	VBAT3	Muti-function IO with wake-up function
2	P0_1	IO	VBAT3	Muti-function IO with wake-up function
3	P0_2	IO	VBAT3	Muti-function IO with wake-up function
4	P0_3	IO	VBAT3	Muti-function IO with wake-up function
5	RST_N/P3_0	IO	VBAT3	Default to system reset, active low The reset function can be disabled by configuring it. Muti-function IO with wake-up function
6	P3_1	IO	VBAT3	Muti-function IO with wake-up function
7	P2_1	IO	VBAT3	Muti-function IO with wake-up function
8	USBDP/P2_7	IO	VBAT3	Default to USB_DP Muti-function IO with wake-up function
9	USBDM/P2_6	IO	VBAT3	Default to USB_DM Muti-function IO with wake-up function
10	P1_7	IO	VBAT3	Muti-function IO with wake-up function SAR-ADC,AIN7
11	VDD18	DP		Flash power & SAR-ADC reference voltage 1.8V power output, connect to capacitor
12	VDD09	AP		Digital logic 0.9V power output, connect to capacitor

13	ONOFF/P4_4	I	VBAT3	ONOFF Key with wake-up function Only GPI
14	SW	AP		DC-DC buck switch
15	VDD12	DP		DC-DC buck 1.2V power output, connect to capacitor
16	IR/P4_3	IO	VBAT3	Infrared signal TX and RX port Only GPIO
17	VBAT3	AP		3V Battery or DC power input,VBAT5 pin can be suspended 2.5V power for efuse
18	VBAT5	AP		5V Battery or DC power input,VBAT3 pin is the output of internal LDO
19	P1_6	IO/AI	VBAT3	Muti-function IO with wake-up function SAR-ADC,AIN6
20	JTAG_TCK/P1_3	IO/AI	VBAT3	Default to JTAG_TCK Muti-function IO with wake-up function SAR-ADC,AIN3
21	JTAG_TMS/P1_2	IO/AI	VBAT3	Default to JTAG_TMS Muti-function IO with wake-up function SAR-ADC,AIN2
22	VIP/P0_4	AI/IO	VBAT3	Default to Audio ADC input, P port Muti-function IO with wake-up function
23	VIN/P4_0	AI/IO	VBAT3	Default to Audio ADC input, N port Only GPIO
24	MICBIAS/P4_1	AP/IO	VBAT3	Bias Voltage for Microphone Only GPIO

25	AVDD25	AP		Analog 2.5V power output, connect to capacitor
26	UART0_RX/P0_5	IO	VBAT3	Default to UART0_RX Muti-function IO with wake-up function
27	UART0_TX/P0_6	IO	VBAT3	Default to UART0_TX Muti-function IO with wake-up function
28	BOOT/P0_7	AI/IO	VBAT3	Default to BOOT Muti-function IO with wake-up function
29	XIN	I		32MHz crystal input
30	XOUT	O		32MHz crystal output
31	VCC_RF	AP		Buck input for RF power
32	RF	AI/AO		RF antenna
33	GND	AG		EPAD ground

3.4. GX8301B pin map

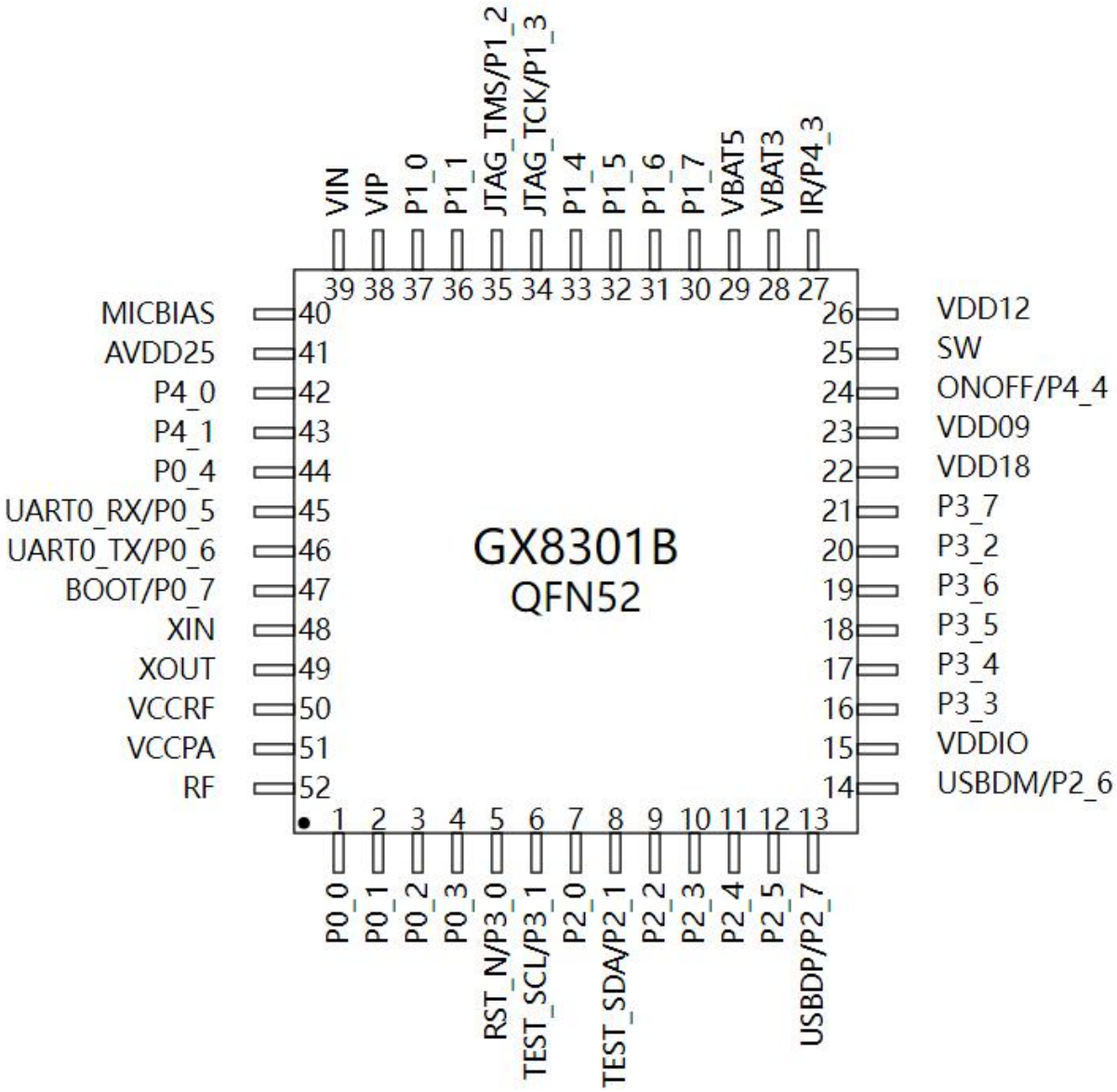


Figure 3.2 GX8301B Pin map

3.5. GX8301B pin description

Pin Number	Pin Name	Type	Domain	Description
1	P0_0	IO	VDDIO	Muti-function IO with wake-up function
2	P0_1	IO	VDDIO	Muti-function IO with wake-up function
3	P0_2	IO	VDDIO	Muti-function IO with wake-up function
4	P0_3	IO	VDDIO	Muti-function IO with wake-up function
5	RST_N/P3_0	IO	VDDIO	Default to system reset, active low The reset function can be disabled by configuring it. Muti-function IO with wake-up function
6	P3_1	IO	VDDIO	Muti-function IO with wake-up function
7	P2_0	IO	VDDIO	Muti-function IO with wake-up function
8	P2_1	IO	VDDIO	Muti-function IO with wake-up function
9	P2_2	IO	VDDIO	Muti-function IO with wake-up function
10	P2_3	IO	VDDIO	Muti-function IO with wake-up function
11	P2_4	IO	VDDIO	Muti-function IO with wake-up function
12	P2_5	IO	VDDIO	Muti-function IO with wake-up function
13	USBDP/P2_7	IO	VDDIO	Default to USB_DP Muti-function IO with wake-up function
14	USBDM/P2_6	IO	VDDIO	Default to USB_DM Muti-function IO with wake-up function

15	VDDIO	DP		GPIO power output, connect to capacitor
16	P3_3	IO	VDDIO	Muti-function IO with wake-up function
17	P3_4	IO	VDDIO	Muti-function IO with wake-up function
18	P3_5	IO	VDDIO	Muti-function IO with wake-up function
19	P3_6	IO	VDDIO	Muti-function IO with wake-up function
20	P3_2	IO	VDDIO	Muti-function IO with wake-up function
21	P3_7	IO	VDDIO	Muti-function IO with wake-up function
22	VDD18	AP		Flash power & SAR-ADC reference voltage 1.8V power output, connect to capacitor
23	VDD09	DP		Digital logic 0.9V power output, connect to capacitor
24	ONOFF/P4_4	I	VBAT3	ONOFF Key with wake-up function Only GPI
25	SW	AP		DC-DC buck switch
26	VDD12	DP		DC-DC buck 1.2V power output, connect to capacitor
27	IR/P4_3	IO	VBAT3	Infrared signal TX and RX port Only GPIO
28	VBAT3	AP		3V Battery or DC power input,VBAT5 pin can be suspended 2.5V power for efuse
29	VBAT5	AP		5V Battery or DC power input,VBAT3 pin is the output of internal LDO

30	P1_7	IO/AI	VDDIO	Muti-function IO with wake-up function SAR-ADC,AIN7
31	P1_6	IO/AI	VDDIO	Muti-function IO with wake-up function SAR-ADC,AIN6
32	P1_5	IO/AI	VDDIO	Muti-function IO with wake-up function SAR-ADC,AIN5
33	P1_4	IO/AI	VDDIO	Muti-function IO with wake-up function SAR-ADC,AIN4
34	JTAG_TCK/P1_3	IO/AI	VDDIO	Default to JTAG_TCK Muti-function IO with wake-up function SAR-ADC,AIN3
35	JTAG_TMS/P1_2	IO/AI	VDDIO	Default to JTAG_TMS Muti-function IO with wake-up function SAR-ADC,AIN2
36	P1_1	IO/AI	VDDIO	Muti-function IO with wake-up function SAR-ADC,AIN1
37	P1_0	IO/AI	VDDIO	Muti-function IO with wake-up function SAR-ADC,AIN0
38	VIP	AI		Default to Audio ADC input, P port
39	VIN	AI		Default to Audio ADC input, N port
40	MICBIAS	AP		Bias Voltage for Microphone
41	AVDD25	AP		Analog 2.5V power output, connect to capacitor
42	P4_0	IO	VDDIO	GPIO

43	P4_1	IO	VDDIO	GPIO
44	P0_4	IO	VDDIO	Muti-function IO with wake-up function
45	UART0_RX/P0_5	IO	VDDIO	Default to UART0_RX Muti-function IO with wake-up function
46	UART0_TX/P0_6	IO	VDDIO	Default to UART0_TX Muti-function IO with wake-up function
47	BOOT/P0_7	AI/IO	VDDIO	Default to BOOT Muti-function IO with wake-up function
48	XIN	I		32MHz crystal input
49	XOUT	O		32MHz crystal output
50	VCC_RF	AP		Buck input for RF power
51	VCC_PA	AP		Buck input for RF PA power,Optional input from external sources
52	RF	AI/AO		RF antenna
53	GND	AG		EPAD ground

3.6. PIN multiplex map

The GPIO of GX8301 is designed with the matrix mechanism of full function reuse.Each GPIO with general multiplexing function can be reused into the function of a peripheral module.

Table 3.5 IO Function List

NUM	FUNC	NUM	FUNC	NUM	FUNC	NUM	FUNC
0	IDLE	1	GPIOn	2	UART0_TX	3	UART0_RX
4	UART0_CTS	5	UART0_RTS	6	UART1_TX	7	UART1_RX
8	UART1_CTS	9	UART1_RTS	10	I2C0_SCL	11	I2C0_SDA
12	I2C1_SCL	13	I2C1_SDA	14	I2C2_SCL	15	I2C2_SDA
16	PWM0	17	PWM1	18	PWM2	19	PWM3
20	PWM4	21	PWM5	22	PWM6	23	PWM7
24	QUAD_X_A	25	QUAD_X_B	26	QUAD_Y_A	27	QUAD_Y_B
28	QUAD_Z_A	29	QUAD_Z_B	30	KEY_COL_0	31	KEY_COL_1
32	KEY_COL_2	33	KEY_COL_3	34	KEY_COL_4	35	KEY_COL_5
36	KEY_COL_6	37	KEY_COL_7	38	KEY_COL_8	39	KEY_COL_9
40	KEY_COL_10	41	KEY_COL_11	42	KEY_COL_12	43	KEY_COL_13
44	KEY_COL_14	45	KEY_COL_15	46	KEY_COL_16	47	KEY_COL_17
48	KEY_COL_18	49	KEY_COL_19	50	KEY_ROW_0	51	KEY_ROW_1
52	KEY_ROW_2	53	KEY_ROW_3	54	KEY_ROW_4	55	KEY_ROW_5
56	KEY_ROW_6	57	KEY_ROW_7	58	KEY_ROW_8	59	KEY_ROW_9
60	KEY_ROW_10	61	KEY_ROW_11	62	SPI2_CS0 (Master)	63	SPI2_CS1 (Master)
64	SPI2_CS2 (Master)	65	SPI1_CLK (Master)	66	SPI1_D0 (Master)	67	SPI1_D1 (Master)
68	SPI1_D2 (Master)	69	SPI1_D3 (Master)	70	SPI1_CS (Master)	71	SPI2_CLK (Master)
72	SPI2_D0 (Master)	73	SPI2_D1 (Master)	74	SPI2_D2 (Master)	75	SPI2_D3 (Master)
76	SPI2_CS (Slave)	77	SPI2_CLK (Slave)	78	SPI2_D0 (Slave)	79	SPI2_D1 (Slave)
80	SPI2_D2 (Slave)	81	SPI2_D3 (Slave)	82	I2S_BCLK (Master)	83	I2S_LRCLK (Master)
84	I2S_DIN	85	I2S_DOUT	86	I2S_BCLK (Slave)	87	I2S_LRCLK (Slave)
88	SD_CLK	89	SD_CMD	90	SD_D0	91	SD_D1
92	SD_D2	93	SD_D3	94	--	95	MCLK
96		97	JTAG_TMS	98	JTAG_CK	99	
100		101	PDM_CLK	102	PDM0_DATA	103	PDM1_DATA
104	--	105	--	106	--	107	--
108	--	109	--	110	--	111	PWM_P
112	PWM_N	113	SD_CARDDETECT	114	--	115	--
116	--	117	SD_WP	118	--	119	--
120	--	121	--	122	--	123	--
124	--	125	--	126	--	127	--

4. Function description

4.1. Bluetooth Features

- Bluetooth Low Energy V5.4 qualified
- Support BLE1M, BLE2M, 125K and 500K coded PHY
- Support all BLE states and all roles (Broadcaster, Central, Observer,Peripheral)
- Support all BLE Audio features, including ISOAL, BIS, CIS, etc
- Advertising Extension
- Support 2.4G proprietary mode
- Max TX Power: 7dBm
- RX sensitivity:-96dBm@BLE1M,-93dBm@BLE2M,-101.5dBm@125K

4.2. CPU

- 32bit RISC-V CPU (T-Head E906), compliant with RV32IMAC[F][D][P]
- 5 stage pipeline, with FPU and DSP units
- Integrated 16KB I-Cache and 4KB D-Cache
- Frequency up to 96 MHz, support DVFS
- 2.0 DMIPS/MHz, 3.6 Coremark/MHz
- Support MP3, SBC, ADPCM, OPUS, LC3 audio decode and encode
- Support RTOS

4.3. Memory

- Internal 128KB SRAM, 80KB of which are capable of entering retention state in deep sleep mode
- Support external PSRAM, which can be accessed by QSPI interface
- SIP 512KB or 1MB QSPI nor flash
- Flash can be programed by UART or USB from scratch

- 256 bits EFUSE memory, with unique ID supported

4.4. Clock

- 32MHz external crystal
- Integrated internal 32KHz and 32MHz OSC
- Integrated PLL for system, audio and USB applications

4.5. Reset

- Integrated power on reset & brown out reset
- Dedicated reset pin

4.6. Audio

- 16bit low-power Sigma-delta ADC, with SNR > 90dB, Dynamic range 92dB
- Suport selection of low-power and high performance modes
- Analog PGA support 0~32dB, with 2dB per step
- 2 channel PDM microphone interface
- Support audio input with sample rate 96k/48k/32k/16k Hz
- I2S input and output interface, support master and slave modes, support TDM x4 mode, support 5-line in-out mode
- Mono channel PWM type audio DAC integrated

4.7. Key Scan

- Matrix key scan mode:

  Up to 12 rows and 20 columns

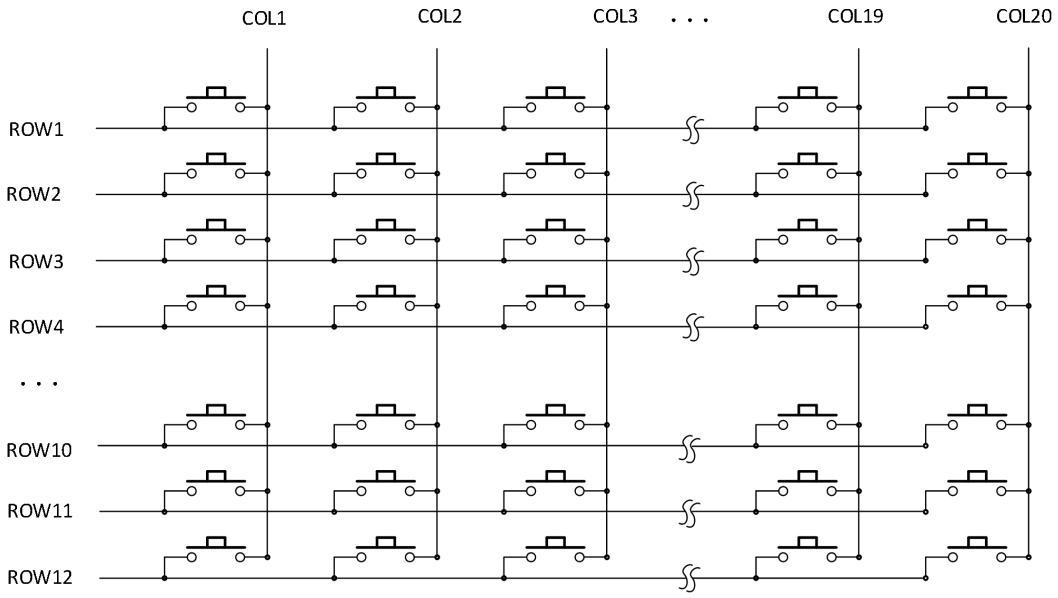


Figure 4.1 matrix key scan

- Determinant key scan mode:

  Up to 31 rows and 31 columns

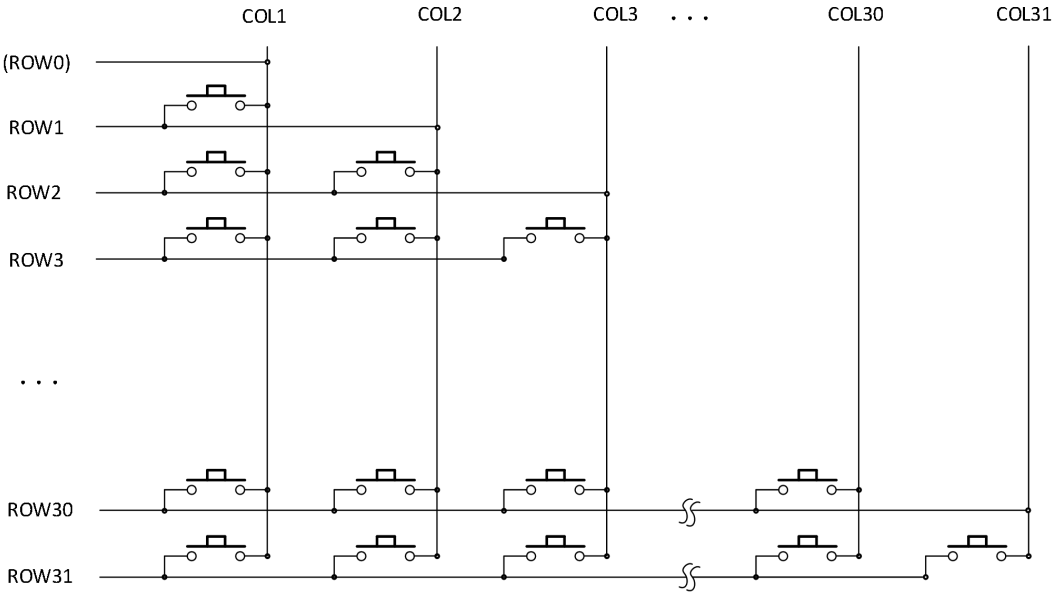


Figure 4.2 determinant key scan

4.8. SPI

- SPI-0 for flash controller, support QSPI, max frequency 96MHz,SIP flash max 85MHz
- SPI-1 QSPI master, can used for LCD driver or PSRM, frequency up to 48MHz
- SPI-2 QSPI master or slave with 3 CS signal, when work at master mode can connect to 3 external SPI devices

4.9. SDIO

- SDIO master, can connect to SD/eMMC cards

4.10. UART

- Integrates 2 UART controllers
- Full-duplex operation
- Supports speed up to 3Mbps
- Supports modem flow control by software or hardware

4.11. I2C

- Integrates 3 I2C controllers
- Support master mode and slave mode
- Support Normal-mode,100kbit/s
- Support Fast-mode,400kbit/s
- Support Fast-mode Plus,1Mbit/s

4.12. GPIO & PWM

- Support maximum 20 GPIOs for QFN32 package, 32 GPIOs for QFN52 package
- Support maximum 8 PWMs
- Each IO independently supports interrupts
- Each IO supports function reuse,please check the function reuse tabel

4.13. Timer, WDT and RTC

- Eight general purpose timer
- Watch dog timer
- RTC timer

4.14. DMA

- AHB bus architecture,4 groups of 32 bits AHB master bus
- Support 4 channels, 32bytes FIFO depth
- Support half duplex and full duplex

4.15. Quadrate decoder

- Support maximum 3 channels independently
- Independent three-axis quadrature decoder
- Sample rate programmable

4.16. USB Slave

- USB 2.0 Full Speed slave
- Support USB Audio, compliant to UAC 1.0 protocol
- Suport USB HID, USB UART
- Support program flash by USB

4.17. Security

- Integrated EFUSE memory, support unique chip id, provide 8bytes for customer use
- Integrated TRNG module
- Integrated AES engine

4.18. Infra-red transmitter and receiver

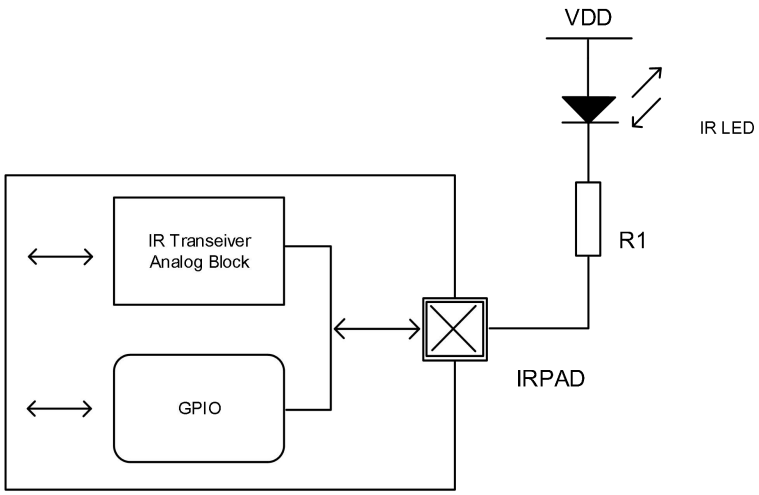


Figure 4.3 Block diagram of Infrared

- Infra-red modulator and demodulator
- Support IR transmit and receive by one port
- Maximum output current is 470mA
- Fixed mode, for standard protocols: 9012\NEC(8bits)\RC5\RC6
- Programmable mode, for non standard protocols

4.19. SAR-ADC

- 12bit SAR-ADC for low speed analog signal sensing.
- Support maximum 4MHz sampling rate

4.20. Power management

4.20.1.Power supply map

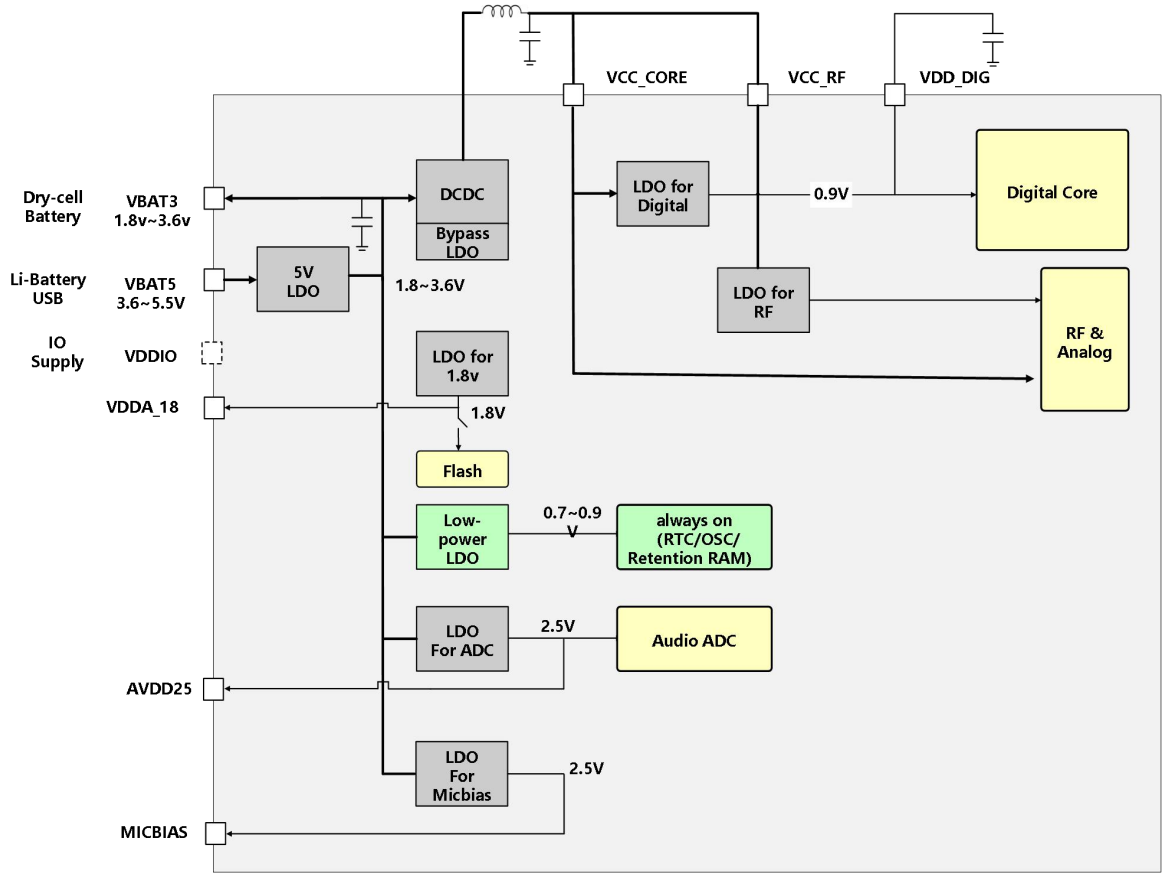


Figure 4.4 GX8301 power supply map

4.20.2.Power Mode

- Ship Mode
- Deep Sleep Mode
- Sleep Mode
- Active Mode

4.20.3.POR&BOR

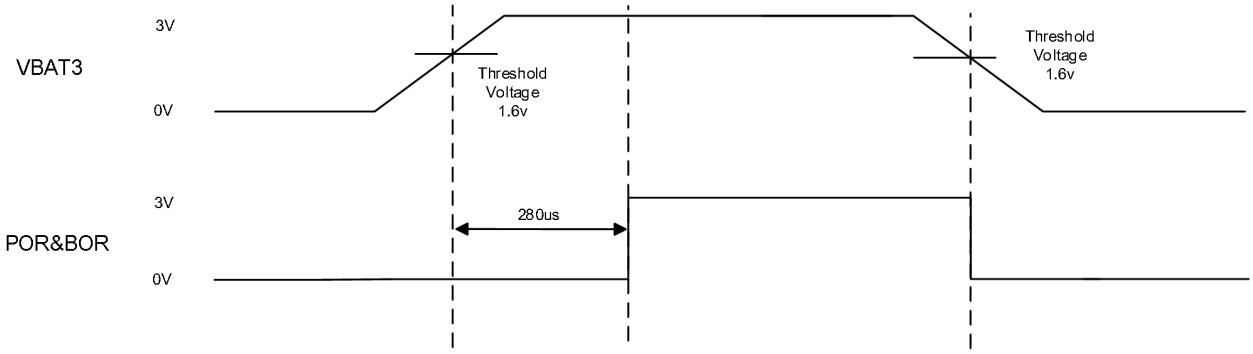


Figure 4.5 POR&BOR

4.21. Power consumption

4.21.1 Sleep Mode power consumption

Table 4.1 Sleep Mode power consumption（ VBAT3=3.0V,25℃ ）

Symbol	Description	Min.	Typ.	Max.	Units
I_{Ship}	Ship Mode, only wake up with power button		0.25		uA
I_{Key}	Deep Sleep Mode, GPIO or key scan wake-up, no SRAMRET, no RTC		0.85		uA
$I_{Key,SRAM}$	Deep Sleep Mode, GPIO or key scan wake-up, 80KB SRAM RET, RTC non wake-up,		1.3		uA
$I_{Key,SRAM,RTC}$	Deep Sleep Mode, GPIO or key scan wake-up, 80KB SRAM RET, RTC wake-up		1.55		uA
I_{Sleep}	Sleep Mode, (VDD09=1.0V,VDD12=1.15V,DCDC work)		0.8		mA

4.21.2 System operating power consumption

Table 4.2 System operating power consumption（Condition: DCDC working）

Symbol	Description	Total power consumption (@VBAT3=3V,Typ.)			Units
		VDD09= 0.9V	VDD09= 1.0V	VDD09= 1.1V	
$I_{MCU96M,LL}$	Fout=MCU=96M, light load	N/A	3.25	3.55	mA
$I_{MCU96M,CM}$	Fout=MCU=96M，run Coremark	N/A	4.78	5.19	mA
$I_{MCU48M,LL}$	Fout=MCU=48M, light load	2.16	2.30	2.46	mA
$I_{MCU48M,CM}$	Fout=MCU=48M，run Coremark	2.81	3.04	3.28	mA
$I_{MCU24M,LL}$	Fout=MCU=24M, light load	1.69	1.81	1.92	mA
$I_{MCU24M,CM}$	Fout=MCU=24M，run Coremark	2.02	2.17	2.32	mA
$I_{Unit,LL}$	Unit frequency power consumption of light loads	17	19	21.5	uA/MHz
$I_{Unit,CM}$	Unit frequency power consumption of Coremark	29	24.5	38	uA/MHz

4.21.3 Bluetooth power consumption

Table 4.3 Bluetooth module power consumption

Symbol	Description	Min.	Typ.	Max.	Units
I_{RX}	Full time reception power consumption, receive maximum gain level①		6.3		mA
$I_{TX@0dB}$	Full time transmission power consumption,@0dB②		7		mA
$I_{TX@6dB}$	Full time transmission power consumption,@6dB③		11		mA

Notes：

①②③Condition: VCCPA=VCCRF=1.2V,measure current at 1.2V

Table 4.4 Sniff chip power consumption

Symbol	Description	Min.	Typ.	Max.	Units
I_{Sniff}	Sniff Mode power consumption@VBAT3=3.0V, DCDC BUCK working, Tsniff=500ms		30		uA

4.21.4 Audio ADC full time power consumption

Table 4.5 Audio ADC full time power consumption@VBAT3

Symbol	Description	Min.	Typ.	Max.	Units
I_{ADC}	ADC power consumption		500		uA
I_{MIC}	MIC power consumption		200		uA
I_{Total}	Total power consumption		700		uA

5. Applications

5.1. Bluetooth voice remote controller

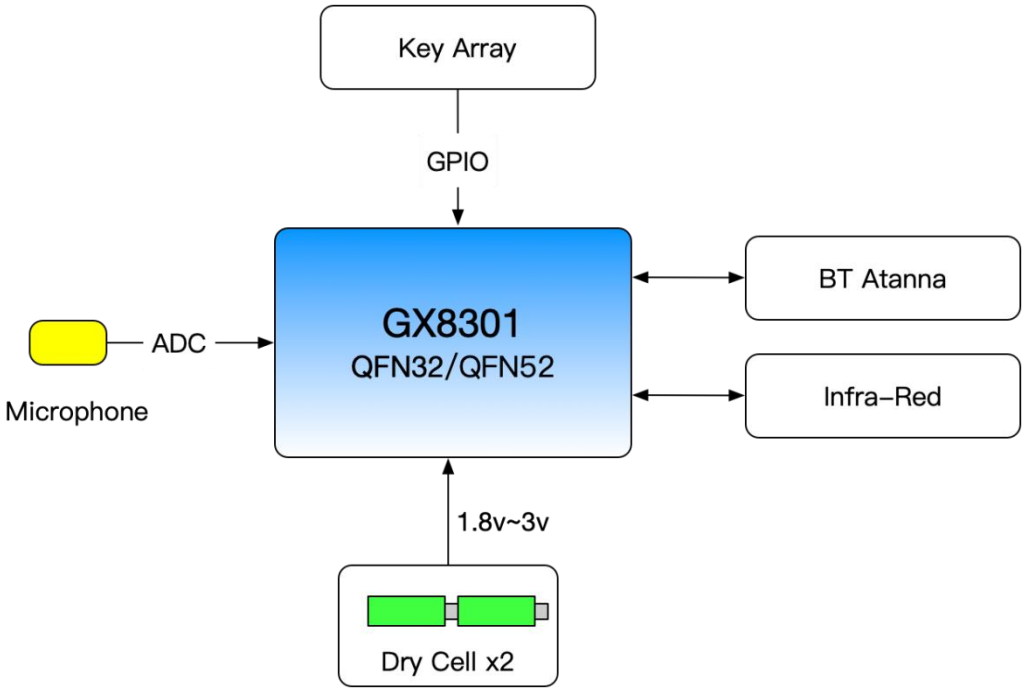


Figure 5.1 Classic GX8301 Application diagram

5.2. BLE USB Dongle

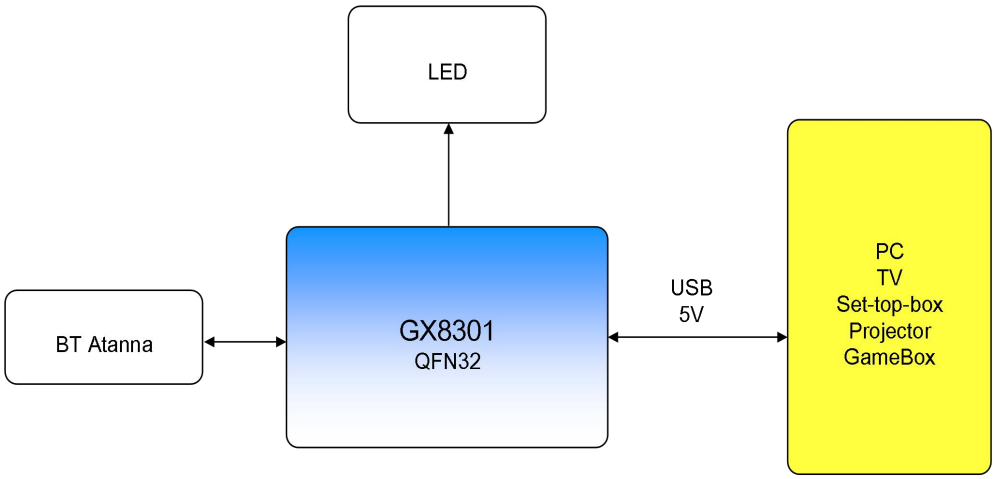


Figure 5.2 BLE USB Dongle

5.3. Low power BLE MCU

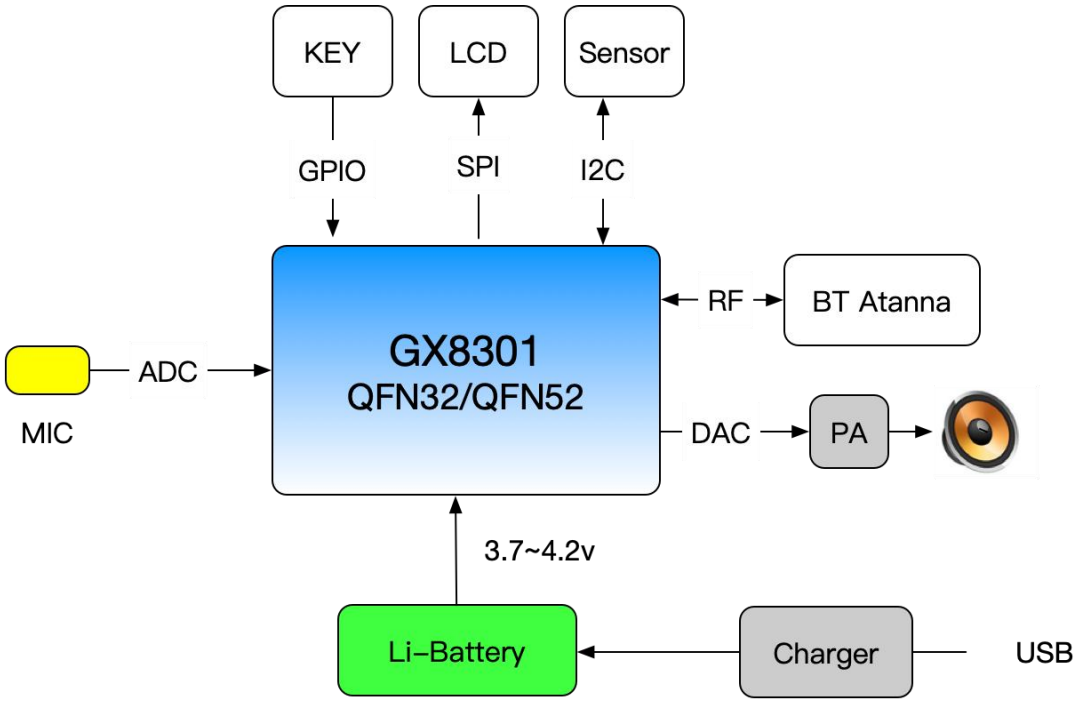


Figure 5.3 Low-power IoT MCU with BLE and audio

6. Electronic specification

6.1. Recommended operating condition

Table 6.1 Recommended operating condition

Parameters	Min	Typ	Max	Units
VBAT5 power supply voltage	3.6	5	5.5	V
VBAT3 power supply voltage	1.8	3	3.6	V
IO Voltage(VDD_IO)	Same with VBAT3			V
Output High Level (VOH)	2.4			V
Output Low Level (VOL)			0.4	V
Input High Level (VIH)	2.0		VDD_IO +0.3V	V
Input Low Level (VIL)	-0.3		0.8	V
Input Leakage Current			±10	uA
Pull-up Resistor	27K	40K	65K	Ω
Storage Temperature	-65		150	℃
Operating Ambient Temperature	-40		85	℃

6.2. RF performance

Table 6.2 RF Receiver performance

BLE	Condition	BT SPEC	GX8301			
Parameter			**Unit**	**Min**	**Typ**	**Max**
Frequency Range			MHz			
Maximum received signal	PER < 30.8%	-10	dBm		0	
for BLE - 1Mbps						
Sensitivity with dirty transmitt off	PER < 30.8%	/	dBm		-96	
Sensitivity with dirty transmitt on	PER < 30.8%	-70	dBm		-95.5	
C/I co-channel	Desired Signal@-67dBm	21	dB		7	
Adjacent channel selectivity C/I (Wanted signal - 67dBM)	F = F0 + 1MHz	15	dB		-1	
	F = F0 - 1MHz	15	dB		4	
	F = F0 + 2MHz	-17	dB		-28	
	F = F0 - 2MHz	-17	dB		-24	
	F = F0 + 3MHz	-27	dB		-31	
	F = F0 - 3MHz	-27	dB		-28	
Image channel selectivity C/I	F = Fimage(F0 - 4MHz)	-9	dB		-28	
Image Aajacnet Channel selectivity C/I	F = Fimage + 1MHz	-15	dB		-28	
	F = Fimage - 1MHz	-15	dB		-35	
Out-of-band blocking performance	30MHz - 2000MHz	-30	dBm			
	2000MHz - 2400MHz	-35	dBm			
	2500MHz - 3000MHz	-35	dBm			
	3000MHz - 12.5GHz	-30	dBm			
Intermodulation						
for BLE - 2Mbps						
Sensitivity with dirty transmitt off	PER < 30.8%	/	dBm		-93	
Sensitivity with dirty transmitt on	PER < 30.8%	-70	dBm		-92.5	
Maximum received signal	PER < 30.8%	-10	dB			
C/I co-channel		21	dB		9	
Adjacent channel selectivity C/I	F = F0 + 2MHz	15	dB		-3	
	F = F0 - 2MHz	15	dB		-1	
	F = F0 + 4MHz	-17	dB		-30	
	F = F0 - 4MHz	-17	dB		-25	

	F = F0 + 6MHz	-27	dB		-32	
	F = F0 - 6MHz	-27	dB		-36	
Image channel selectivity C/I	F = Fimage(F0 - 4MHz)-2M	-9	dB		-36	
Image Aajacnet Channel selectivity C/I	F = Fimage -2M + 2MHz	-15	dB		-25	
	F = Fimage -2M - 2MHz	-15	dB		-37	
Out-of-band blocking performance	30MHz - 2000MHz	-30	dBm			
	2000MHz - 2400MHz	-35	dBm			
	2500MHz - 3000MHz	-35	dBm			
	3000MHz - 12.5GHz	-30	dBm			
Intermodulation						
for BLE LR 500K						
Sensitivity with dirty transmitt off	PER < 30.8%	/	dBm		-98.5	
Sensitivity with dirty transmitt on	PER < 30.8%	-75	dBm		-98	
C/I co-channel	Desired Signal@-72dBm	17	dB		3	
Adjacent channel selectivity C/I (Wanted signal - 67dBM)	F = F0 + 1MHz	11	dB		-3	
	F = F0 - 1MHz	11	dB		-1	
	F = F0 + 2MHz	-21	dB		-31	
	F = F0 - 2MHz	-21	dB		-29	
	F = F0 + 3MHz	-31	dB		-36	
	F = F0 - 3MHz	-31	dB		-31	
Image channel selectivity C/I	F = Fimage(F0 - 4MHz)	-13	dB		-31	
Image Aajacnet Channel selectivity C/I	F = Fimage + 1MHz	-19	dB		-31	
	F = Fimage - 1MHz	-19	dB		-38	
Out-of-band blocking performance	30MHz - 2000MHz	-30	dBm			
	2000MHz - 2400MHz	-35	dBm			
	2500MHz - 3000MHz	-35	dBm			
	3000MHz - 12.5GHz	-30	dBm			
Intermodulation						
for BLE LR 125K						
Sensitivity with dirty transmitt off	PER < 30.8%	/	dBm		-101.5	
Sensitivity with dirty transmitt on	PER < 30.8%	-82	dBm		-101	
C/I co-channel	Desired Signal@-79dBm	12	dB		3	
Adjacent channel selectivity C/I (Wanted signal - 67dBM)	F = F0 + 1MHz	6	dB		-6	
	F = F0 - 1MHz	6	dB		-3	
	F = F0 + 2MHz	-26	dB		-31	
	F = F0 - 2MHz	-26	dB		-33	

	F = F0 + 3MHz	-36	dB		-29	
	F = F0 - 3MHz	-36	dB		-31	
Image channel selectivity C/I	F = Fimage(F0 - 4MHz)	-18	dB		-31	
Image Aajacnet Channel selectivity C/I	F = Fimage + 1MHz	-24	dB		-34	
	F = Fimage - 1MHz	-24	dB		-40	
Out-of-band blocking performance	30MHz - 2000MHz	-30	dBm			
	2000MHz - 2400MHz	-35	dBm			
	2500MHz - 3000MHz	-35	dBm			
	3000MHz - 12.5GHz	-30	dBm			
Intermodulation						

Table 6.3 RF Transmitter performance

BLE - 1Msps	**Condition**	**BT SPEC**	**GX8301**			
Parameters			**Unit**	**Min**	**Typ**	**Max**
Frequency Range			Mhz			
Maximum RF transmit power		/	dBm		7	
RF power control range		/	dB			
Carrier Frequency Offset and Drift	Frequency Offset	[-150, 150]	kHz		6.21	
	Max. Frequency drift	[-50, 50]	kHz		4.52	
	Max. drift rate	≤400	Hz/us		-5.17	
Modulation Characteristic	Δf1avg	[225, 275]	kHz		266.7	
	Δf2 99.9%	≥185	kHz		224.2	
	Δf2avg/Δf1avg	≥0.8	/		0.89	
In-band spurious emissions	+/-2MHz OFFSET	-20	dBm		-43	
	>+/-3MHz offset	-30	dBm		-59	
BLE - 2Msps						
Parameters	**Condition**			**Min**	**Typ**	**Max**
Frequency Range			Mhz			
Maximum RF transmit power		/	dBm		7	
RF power control range		/	dB			
Carrier Frequency Offset and Drift	Frequency Offset	[-150, 150]	kHz		-13.55	
	Max. Frequency drift	[-50, 50]	kHz		5.35	
	Max. drift rate	≤400	Hz/us		-9.46	
Modulation Characteristic	Δf1avg	[450, 550]	kHz		488.4	
	Δf2 99.9%	≥370	kHz		471.2	
	Δf2avg/Δf1avg	≥0.8	/		1.05	
In-band spurious	+/-4MHz OFFSET	-20	dBm		-58	

emissions	+/-5MHz offset	-30	dBm		-59	
	>+/-6MHz offset	-30	dBm		-59	

6.3. ESD

Table 6.4 Electrostatic discharge

Parameters	Min	Max	Units
Human Body Model (HBM)	-2	2	kV
Charged Device Model (CDM)	-500	500	V

6.4. ADC Characteristics

Table 6.5 ADC Characteristics

ADC Parameter						
AVDD=2.5V,VDIG=0.9V,ADC_GAIN=0dB						
Parameter	**Test condition**	**Min**	**Typ**	**Max**	**Unit**	**Describe**
Input Common Mode	-	-	1.25	-	V	
pga_gain	-	-	0~32	-	dB	2dB per step
Full Scale input Voltage	（THD+N=0.2%）	-	4.4	-	Vpp	
Noise	Fs=48KHz A-weighted	-	-92.1	-	dBFS	
SNR	Fs=48KHz A-weighted	-	89.9	-	dBFS	
Dynamic Range	4.4mVpp input (-60dB of max input level) Fs=48KHz A-weighted	-	92	-	dB	
THD	Best at -6dBFS input Fs=48KHz A-weighted	-	-81.1	-	dB	

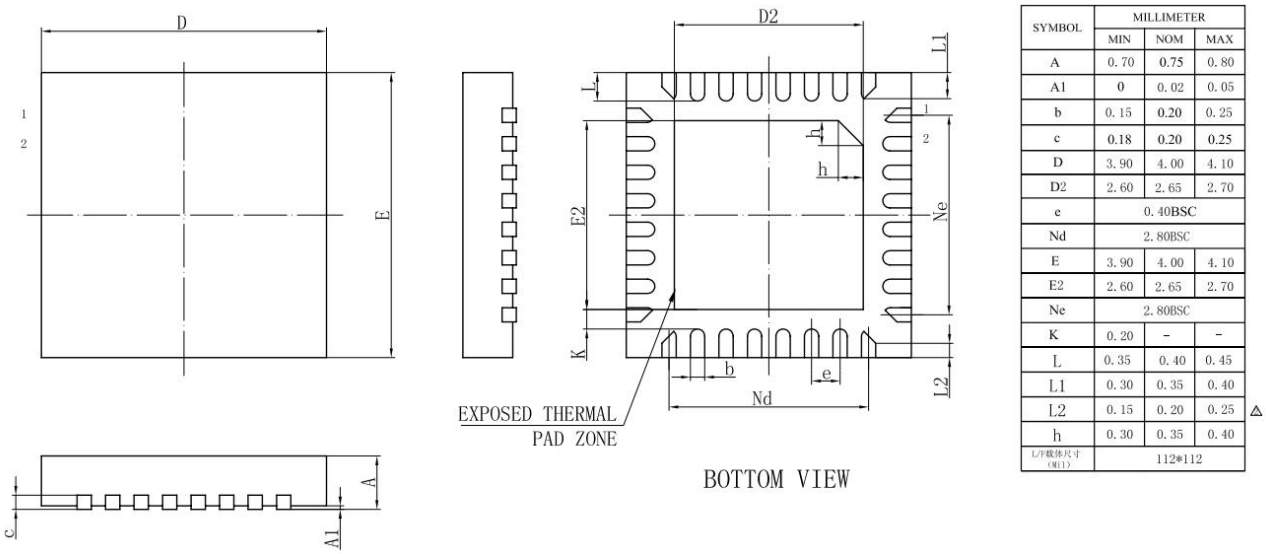
6.5. LoDAC Characteristics

Table 6.6 LoDAC Characteristics

LoDAC Parameter					
LoDAC-3dB attenuation,6.4MHz clock from 32MHz crystal oscillator					
Parameter	**Test condition**	**Min**	**Typ**	**Max**	**Unit**
Noise	0 input		-97		dBu
Digital quantity full amplitude input	1.38Vrms		5.0		dBu
SNR			102		dBFS
THD	sine@1KHz1.38Vrms,200kΩ,A-wt		-85		dB
THD+N	sine@1KHz1.38Vrms,200kΩ,A-wt		-78		dB

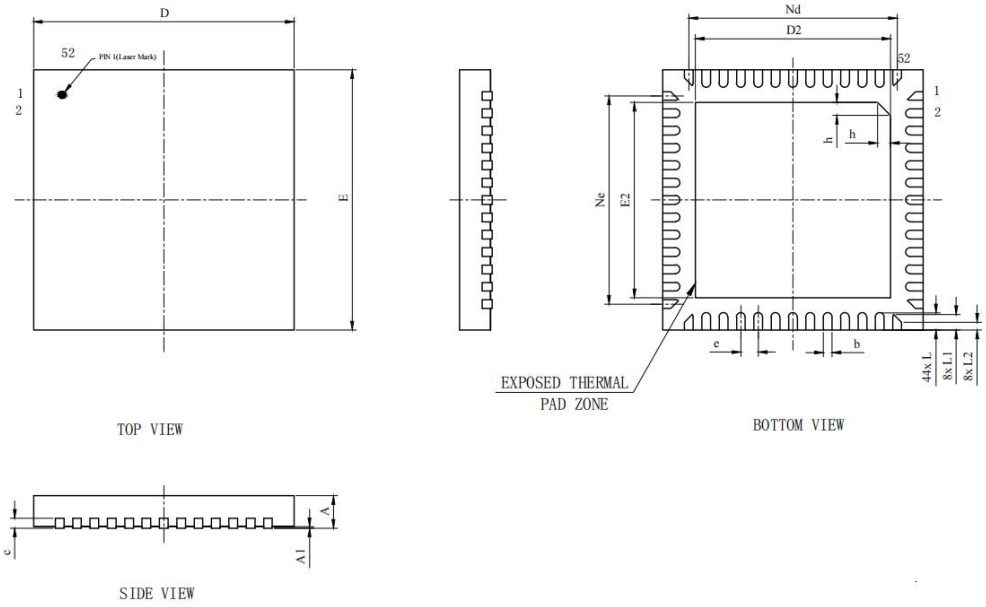
7. Package

7.1. Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
K	0.20	-	-
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
载体尺寸	112*112		

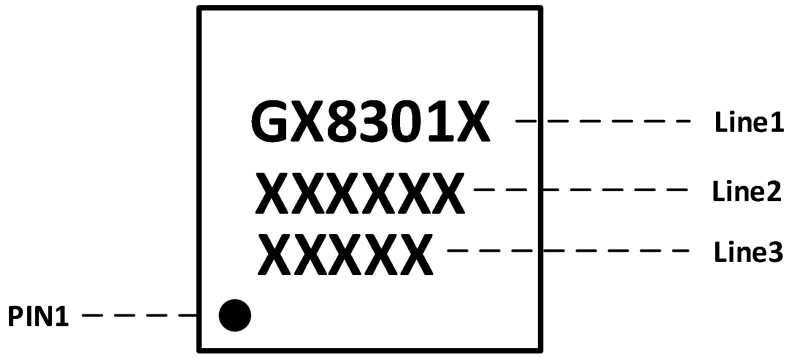
Figure: 7.1 QFN32 Package parameters



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1	—	0.035	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.40	4.50	4.60
e	0.40BSC		
Nd	4.80BSC		
E	5.90	6.00	6.10
E2	4.40	4.50	4.60
Ne	4.80BSC		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F载体尺寸 (mil)	185*185		

Figure: 7.2 QFN52 Package parameters

7.2. Chip mark description



- Line 1: Chip name
- Line 2 : First 6 digit of production lot number
- Line 3 : Last several digit of production lot number
- PIN 1: Pin 1 start point mark

8. Ordering Information

	Flash	PSRAM	Package	MOQ	Other
GX8301A	512KB	none	QFN32	3k	
GX8301B	512KB	none	QFN52	3k	

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