GX8003 Datasheet

High performance AI voice processor

http://www.nationalchip.com

Document Revision History:

Version	Date	Change Log	Author
V0.0	2023.8.17	Initial version	Yun Ling
V0.1	2023.10.19	First release after review	Yun Ling
V0.2	2023.11.28	Modify packaging materials information	Dong Wei
V0.3	2024.8.7	Add Description of the PWM module & PowerOn Delay Parameter	Dong Wei

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1.Features

GX8003 is a high performance and multi-function voice recognition and processing chip. It integrates NationalChip's low-power NPU(Neural Process Unit), 32-bit RISC MCU, ADC/DAC and rich interfaces. It can recognize voice keywords or command words. And it is easy to use and low cost for various IOT applications.

MCU:

- 32-bit low-power RISC CPU with I/D cache and FPU
- Maximum frequency 60MHz

NPU:

- NationalChip's low-power and high-efficient neural processor, gxNPU V200
- Supports popular models such as DNN / CNN / LSTM

Memory:

- Built-in SRAM, size 208KB
- SIP QSPI Nor Flash, size 1MB

Audio ADC:

- Integrated low-power audio ADC
- Programmable gain amplifier, supports 20~32dB gain with 1dB per step

Audio interfaces:

- Dual-channel PDM interface, supports master and slave mode
- Dual-channel Audio DAC output

Communication interfaces:

- Two UARTs
- I2C Master and Salve
- SPI Master /Slave configurable
- Two PWM output ports
- GPIOs

System control:

- Integrates POR(power on reset)
- Internal 32KHz, 24MHz OSC
- No need crystal clock outside

Voltage supply:

- Single power 3.3v supply
- Integrates LDO for core power

Typical power consumption:

- Standby: < 5 mW
- Active: < 30 mW

Note: power measured in 25 degree

Package Type:

- SOP16

2.Chip Architecture

2.1.Block Diagram

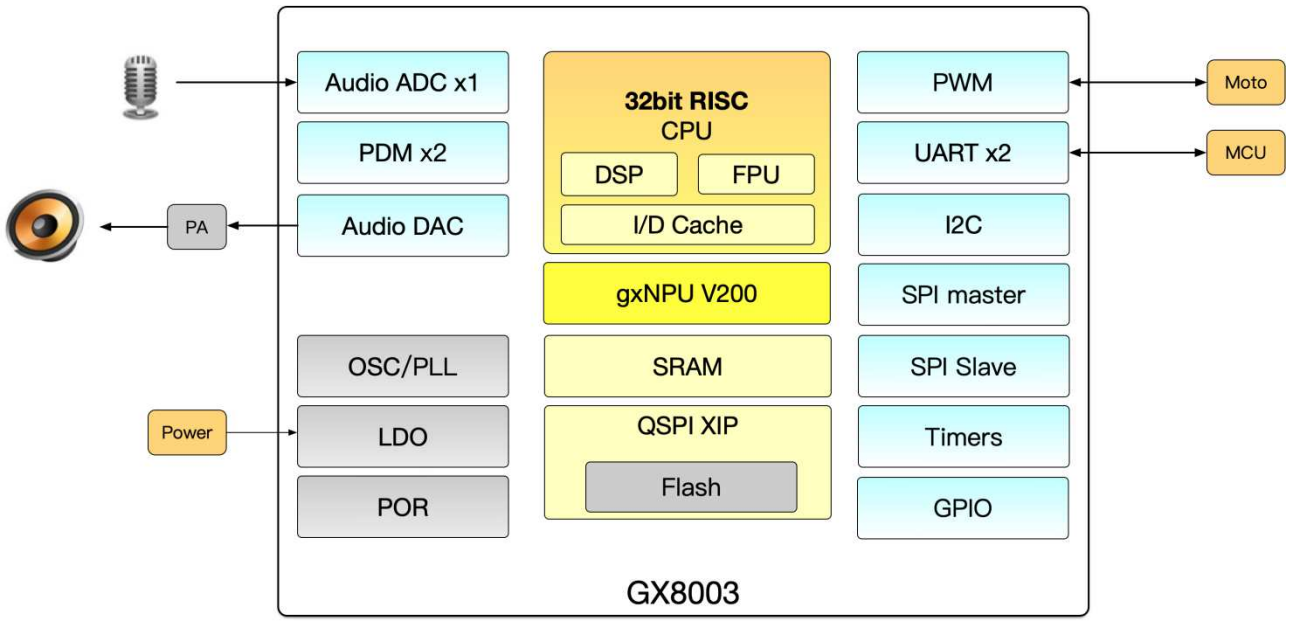


Figure 2- 1 GX8003 chip block diagram

3.Pin Description

3.1.Pin Map

The GX8003 is available in 16-pin SOP16 package.

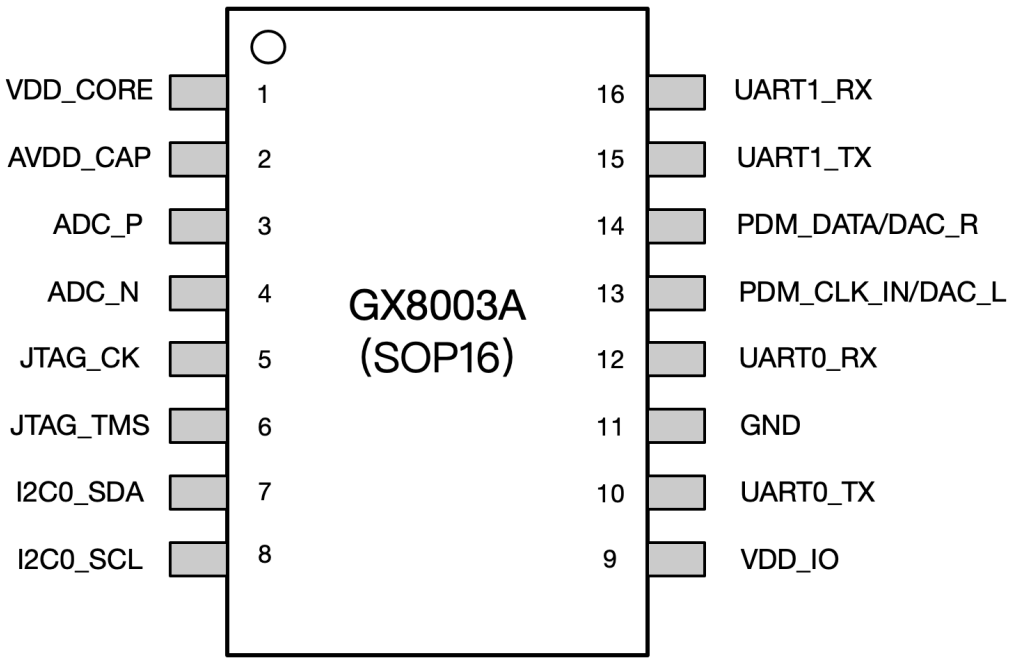


Figure 3- 1 GX8003 pin map

3.2.Acronyms

DP => Digital Power
AP => Analog Power
I => Digital Input
O => Digital Output
IO => Digital Bi-directional
OD => Open Drive
AI => Analog Input
AO => Analog Output

3.3.Pin Multiplexing Functions

Table 3- 1 Pin mux

Pin	Function00	Function01	Function02	Function03	Function04	Function05	Function07
06	JTAG_TMS	GPIO_00			SPI_CSn_M	SPI_CSn_S	PDM_DATA
05	JTAG_CK	GPIO_01			SPI_MISO_M	SPI_MISO_S	PDM_CLK_IN
07	I2C0_SDA	GPIO_03	PDM_CLK_IN	PDM_CLK_OUT			
08	I2C0_SCL	GPIO_04	PDM_DATA				
10	UART0_TX	GPIO_05	I2C1_SDA	PDM_CLK_IN	DAC_OUT_L	PDM_CLK_OUT	
12	UART0_RX	GPIO_06	I2C1_SCL	PDM_DATA	DAC_OUT_R	EXT_CLK_IN	
13	PDM_CLK_IN	GPIO_07			SPI_SCLK_M	SPI_SCLK_S	DAC_OUT_L
14	PDM_DATA	GPIO_08			SPI_MOSI_M	SPI_MOSI_S	DAC_OUT_R
15	UART1_TX	GPIO_11			SPI_SCLK_M	SPI_SCLK_S	DAC_OUT_L
16	UART1_RX	GPIO_12			SPI_MOSI_M	SPI_MOSI_S	DAC_OUT_R

Note:Any GPIO pin of the GX8003 can be configured as **PWM output mode**,the **maximum number** of configurable channels is **2**.

3.4.Power and Analog Pins

Table 3-2 Power and analog pins

Pin Number	Pin Name	Type	Description
9	VDD_IO	DP	Digital IO power
1	VDD_CORE	DP	Digital core power
2	AVDD_CAP	AP	Connect to capacitor for analog power
3	ADC_P	AI	Audio ADC input, P port
4	ADC_N	AI	Audio ADC input, N port

3.5.Multi-function Pins

Table 3-4 Multi-function pins

PIN Number	PIN Name	I/O (Default)	PULL	Function Number	Function Name	Type	Description
7	I2C0_SDA	I	UP	0	I2C0_SDA	IO(OD)	Data of I2C0（Slave)
				1	GPIO_03	IO	General-purpose I/O
				2	PDM_CLK_IN	I	Clk of audio in pdm interface(slave)
				3	PDM_CLK_OUT	O	Clk of audio in pdm interface(Master)
8	I2C0_SCL	I	UP	0	I2C0_SCL	IO(OD)	Clk of I2C0（Slave)
				1	GPIO_04	IO	General-purpose I/O
				2	PDM_DATA	I	Data of audio in pdm interface
10	UART0_TX	O		0	UART0_TX	O	UART0 data transmit
				1	GPIO_05	IO	General-purpose I/O
				2	I2C1_SDA	IO(OD)	Data of I2C1（Master)
				3	PDM_CLK_IN	I	Clk of audio in pdm interface(Slave)
				4	DAC_OUT_L	O	Audio DAC left channel output
				5	PDM_CLK_OUT	O	Clk of audio in pdm interface(Master)

PIN Number	PIN Name	I/O (Default)	PULL	Function Number	Function Name	Type	Description
12	UART0_RX	I		0	UART0_RX	I	UART0 data receive. **Should be fixed value during power up, please add pull-up resister or connect to ground if not using.**
				1	GPIO_06	IO	General-purpose I/O
				2	I2C1_SCL	IO(OD)	Clk of I2C1（Master)
				3	PDM_DATA	I	Dat of audio in pdm interface
				4	DAC_OUT_R	O	Audio DAC right channel output
				5	EXT_CLK_IN	I	External system clock input
13	PDM_CLK_IN	I		0	PDM_CLK_IN	I	Clk of audio in pdm interface(Slave)
				1	GPIO_07	IO	General-purpose I/O
				4	SPI_SCLK_M	O	SCK of SPI interface(Master)
				5	SPI_SCLK_S	I	SCK of SPI interface(Slave)
				7	DAC_OUT_L	O	Audio DAC left channel output
14	PDM_DATA	I		0	PDM_DATA	I	Dat of audio in pdm interface
				1	GPIO_08	IO	General-purpose I/O
				4	SPI_MOSI_M	IO	MOSI of SPI interface(Master)
				5	SPI_MOSI_S	I	MOSI of SPI interface(Slave)
				7	DAC_OUT_R	O	Audio DAC right channel output
15	UART1_TX	O		0	UART1_TX	O	UART1 data transmit
				1	GPIO_11	IO	General-purpose I/O
				4	SPI_SCLK_M	O	SCK of SPI interface(Master)
				5	SPI_SCLK_S	I	SCK of SPI interface(Slave)
				7	DAC_OUT_L	O	Audio DAC left channel output
16	UART1_RX	I		0	UART1_RX	I	UART1 data receive. **Should be fixed value during power up, please add pull-up resister or connect to ground if not using.**
				1	GPIO_12	IO	General-purpose I/O
				4	SPI_MOSI_M	IO	MOSI of SPI interface(Master)
				5	SPI_MOSI_S	I	MOSI of SPI interface(Slave)
				7	DAC_OUT_R	O	Audio DAC right channel output

PIN Number	PIN Name	I/O (Default)	PULL	Function Number	Function Name	Type	Description
6	JTAG_TMS	I		0	JTAG_TMS	IO	MCU Debug interface mode select
				1	GPIO[00]	IO	General-purpose I/O
				4	SPI_CSn_M	O	CSn of SPI interface(Master)
				5	SPI_CSn_S	I	CSn of SPI interface(Slave)
				7	PDM_DATA	I	Data of audio in pdm interface
5	JTAG_CK	I		0	JTAG_CK	I	MCU Debug interface clock
				1	GPIO_01	IO	General-purpose I/O
				4	SPI_MISO_M	I	MISO of SPI interface(Master)
				5	SPI_MISO_S	IO	MISO of SPI interface(Slave)
				7	PDM_CLK_IN	I	Clk of audio in pdm interface(Slave)

4.Function Overview

4.1.CPU Architecture

- 32-bit RISC CPU, frequency up to 60MHz
- Instruction cache 4KB，data cache 8KB
- Supports DSP and FPU acceleration unit
- 32 interrupt sources in total
  - Each interrupt source can be independently enabled
  - Unmasked interrupts can wake up the chip in sleep mode

4.2.Memory

- Integrates 208KB SRAM
- Internally encapsulates 1MB SPI NOR flash in SIP style
  - Supports standard, dual or quad mode of SPI interface
  - Allow to execute code (XIP) directly from the flash
  - SPI clock frequency up to 60MHz

4.3.Clock

- On-chip 32KHz/24MHz oscillator circuit
- One phase-locked loops (PLL) with programmable multiplier up to 60MHz

4.4.NPU

- NationalChip's gxNPU V200, low-power optimized version of neural process unit
- Supports DNN/CNN/DS-CNN/LSTM/GRU and other popular models
- Supports 8-bit quantization, and weights compression
- Compiler supports direct conversion from Tensorflow and Pytorch

4.5.System Peripheral

•I2C

- System I2C Slave: can access system control register, share the ports with I2C0 ports, and work evenly in MCU sleep mode.
- I2C0 : I2C slave, can be used to program flash memory during booting period.
- I2C1 : General purpose I2C controller. Master /slave configurable，
- Chip address configuration: 3 I2C controller has different chip address, you can check the table below.

Table 4- 1 I2C address map

I2C_address	I2C0 PORTS		I2C1 PORTS
	System I2C	I2C0 Slave	I2C1 Slave
During boot stage	0x2F	0x35	0x35
Work Status	0x2F	configurable	configurable

•DMA

- 2 channel DMA
- Supports 8/16/32/64-bit data width
- Supports memory-to-memory, memory-to-peripheral, and peripheral-to-memory data transfer types

•UART

- Integrates 2 UART controllers
- Full-duplex operation
- Supports speed up to 1.5 Mbps
- Supports modem flow control by software or hardware

•SPI Interface

- Master/slave configurable
- Polarity and phase of Chip Select and SPI Clock are configurable

•Timer

- Consists of four 32-bit up-counters

•WDT

- Programmable and hard coded reset pulse length.
- An interrupt is generated first, and if the interrupt is not cleared by the service routine before the second timeout, a system reset is generated
- 32-bit WDT counter

•RTC

- Alarm function – generates an interrupt after a programmed number of cycles
- Configurable option to include the prescaler counter.

4.6.Power Management

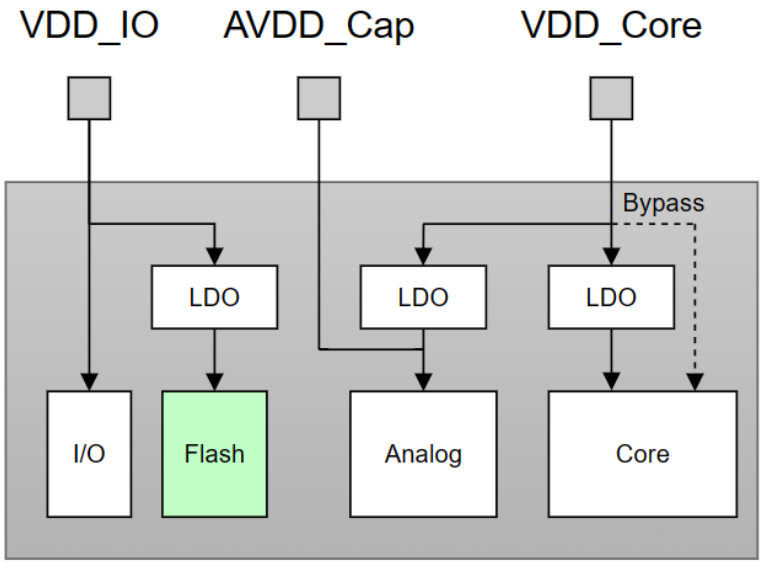


Figure 4- 1 Chip power supply system

•I/O voltage support 1.8v/3.3v

•Core voltage support 1.1v~3.3v

•Integrates two LDO for chip power supply.

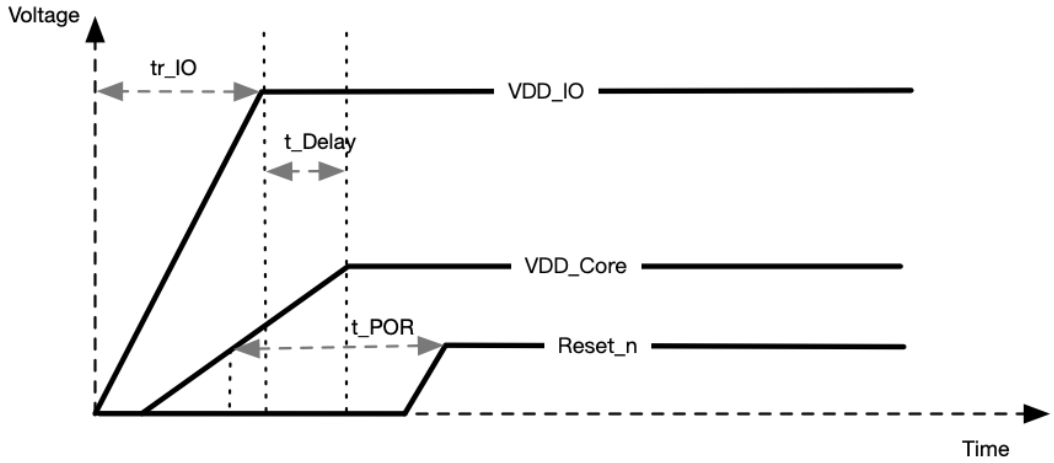
•If the VDD_Core is above 1.2v, please enable internal core LDO.

4.7.Power on and Reset

•System can power on from Flash，I2C and UART。

•During power on or reset the signals of pin UART0_RX and UART1_RX should be fixed value, if you are not using please connect to ground or add pull-up resisters.

•Integrates POR(power on reset) module, the power on sequence should meet the following condition:



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parameter	Description	MIN	MAX	Unit
tr_IO	IO power rise up time	0.02	2	ms
t_Delay	Core power rise up delay time compare with IO power	3		ms
t_IO_Core	the internal flash LDO output	0.02	4	ms
t_POR	Time of POR signal generation after VDD_Core power up to active stage.	4	8	ms

5.Applications

5.1 Typical Applications

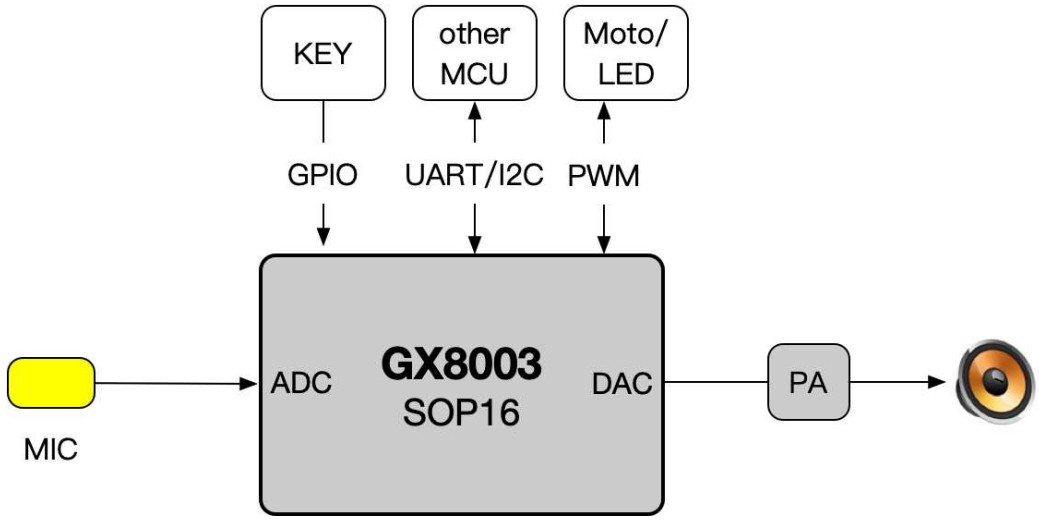


Figure 5- 1 Block diagram of voice enabled IOT device

Key Features:

- Supports PDM and analog type microphone
- Supports voice wake-up, and short voice commands
- Audio play of music or TTS answers
- UART / I2C /SPI communicate with other chips

6.Electronic Specification

6.1.Recommended Operating Condition

Table 6- 1 Recommended operating conditions

Parameters	Min	Typ	Max	Units
IO Power Supply Voltage(VDD_IO)	2.9	3.3	3.6	V
Output High Level (VOH)	2.4			V
Output Low Level (VOL)			0.4	V
Input High Level (VIH)	2.0		VDD_IO +0.3V	V
Input Low Level (VIL)	-0.3		0.8	V
Input Leakage Current			±100	uA
Pull-up Resistor	27K	40K	65K	Ω

Table 6- 2 Recommended operating conditions continue

Parameters	Min	Typ	Max	Units	Remark
VDD_Core Voltage (Bypass internal LDO)	1.0	1.2	1.25	V	
VDD_Core Voltage (Use internal LDO)	1.2	3.3	3.6	V	
Storage Temperature	-40	25	150	℃	
Operating Ambient Temperature	-40	25	85	℃	

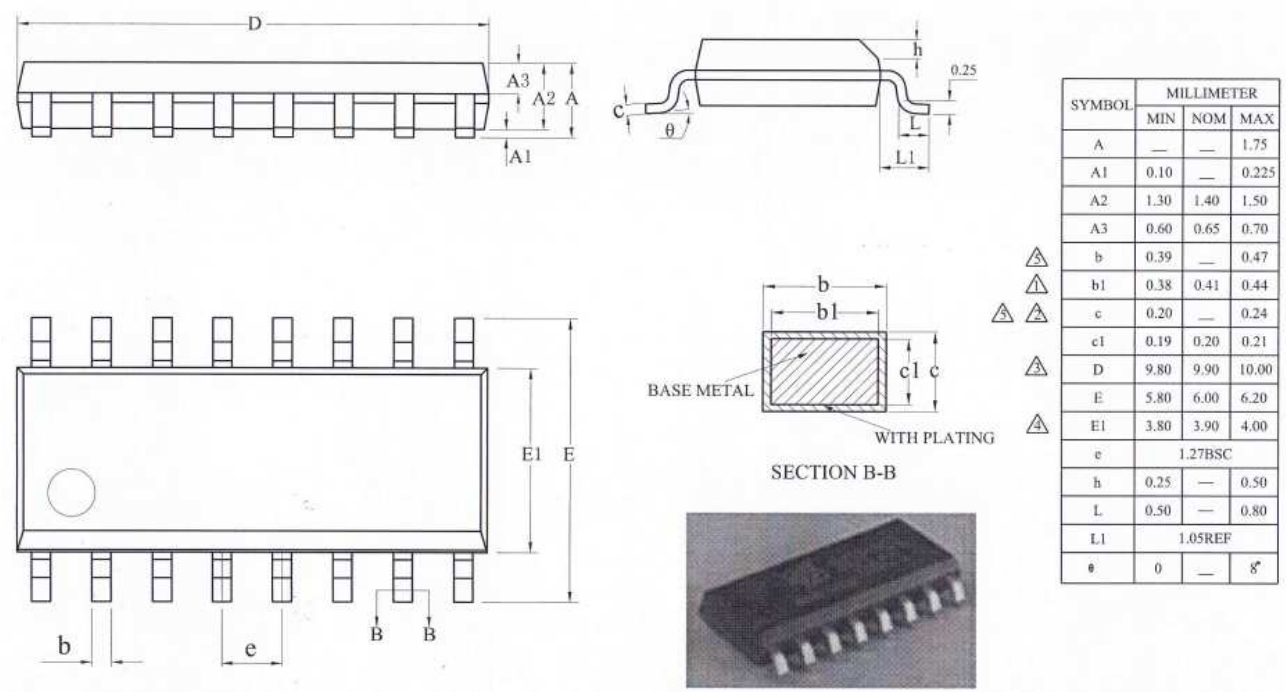
6.2.Electrostatic Discharge

Table 6- 4 Electrostatic discharge

Parameters	Min	Max	Units
Human Body Model (HBM)	-2	2	kV
Machine Model (MM) J ESD22-A115C	-200	200	V

7.Package Information

7.1.Package Specification



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 7- 1 SOP16 package specification

7.2.Chip mark description

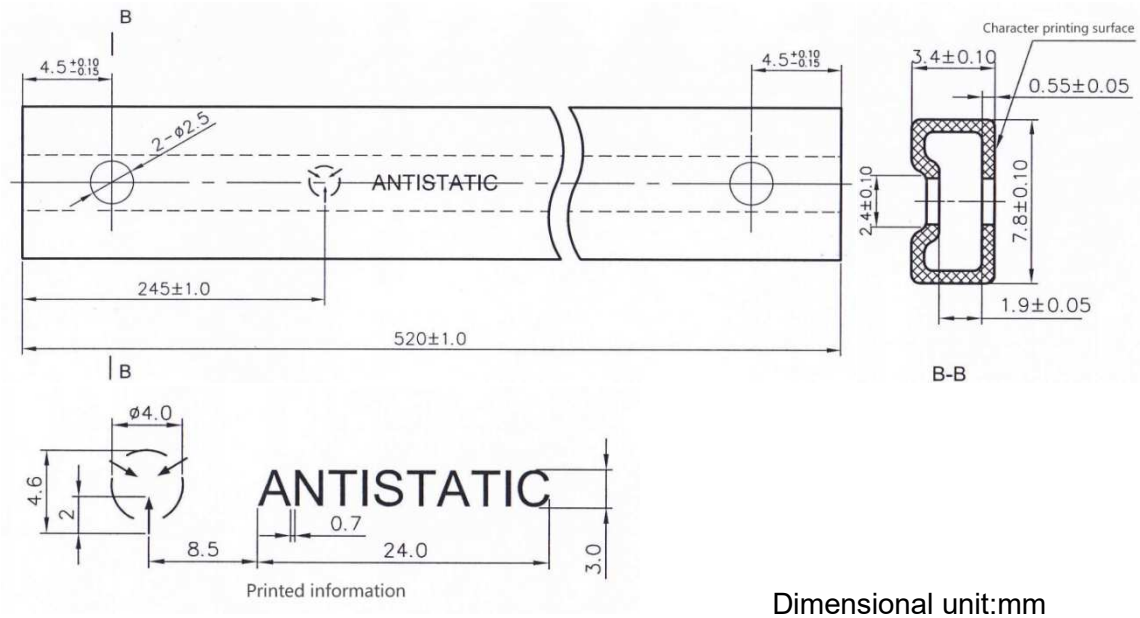
Figure 7- 2 Chip mark description

Description:

- Line 1: Chip name
- Line 2: 10 digit of production lot number
- PIN 1: Pin 1 start point mark

7.3.Package materials Information

1.TUBE



Dimensional unit:mm

Packaging quantity				
Packaging form	Pcs/Tube	Tube/Boxful	Boxful/BOX	Pcs/BOX
SOP16	50	100	10	50000

7.4.Convection Reflow Profile

The test results meet 3 reflow solderings, and the reflow temperature is 260 degrees. The details are as follows:

Table 7- 1 Convection reflow profile

Profile Feature	Note	Pb-Free Assembly
Average ramp-up rate	Tsmax to Tp	0.6~1.5℃/sec
Preheat	-Temperature Min(Tsmin)	150℃
	-Temperature Max(Tsmax)	200℃
	-Time(min to max)(ts)	60-120sec
Time maintained above:	-Temperature(TL)	217℃
	-Time(tL)	60-150 sec

Profile Feature	Note	Pb-Free Assembly
Peak Temperature(Tp)		250±5℃
Time within 5℃ of actual Peak Temperature(tp)		≥30sec
Ramp-down Rate		≤3℃/ sec
Time 25℃ to Peak Temperature		≤8 min

8.Ordering Information

Table 8- 1 Ordering information

Ordering Code	Embedded SPI Nor Flash	Package	MOQ
GX8003A	1MByte	SOP16	5K

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