GX8008C

Smart voice front-end chip

Aug, 2023
Version 2.0

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1. General Introduction

GX8008C is an embedded SoC chip designed for smart voice front-end applications. Targeted at the features of smart voice applications, GX8008C is uniquely designed in a heterogeneous multi-core architecture, and integrates DSP for voice processing, 32-bit RISC MCU for system application, Audio DAC and other peripherals. It enables the product to perform deep neural network computation and various microphone array based on voice signal processing in chip. The chip integrates multi-channel ADC, audio DAC, rich peripheral interfaces as well as an embedded SRAM, which makes its size smaller, power consumption lower, and the entire hardware design simpler.

The highlights of the chip includes following features:

- **MCU**: 32-bit RISC CPU, frequency up to 150MHz, support JTAG
- **DSP**: Tensilica HIFI4 DSP processor, speed up to 400MHz
- **SRAM**:1.5MByte embedded
- **Mic Array**: supports 4 analog or digital mics, both PDM and I2S are supported
- **Audio**: supports analog and digital audio input and direct DAC output
- **VAD**: supports hardware with VAD function for low-power application
- **Flash**: SPI for Nor Flash, with XIP mode
- **Peripherals**: SPI master, 2xI2C,3xUART,8xPWM, USB 2.0 Slave
- **Package**: QFN52,6x6mm
- **Clock**:12MHz crystal

2. Chip Architecture

2.1. Block Diagram

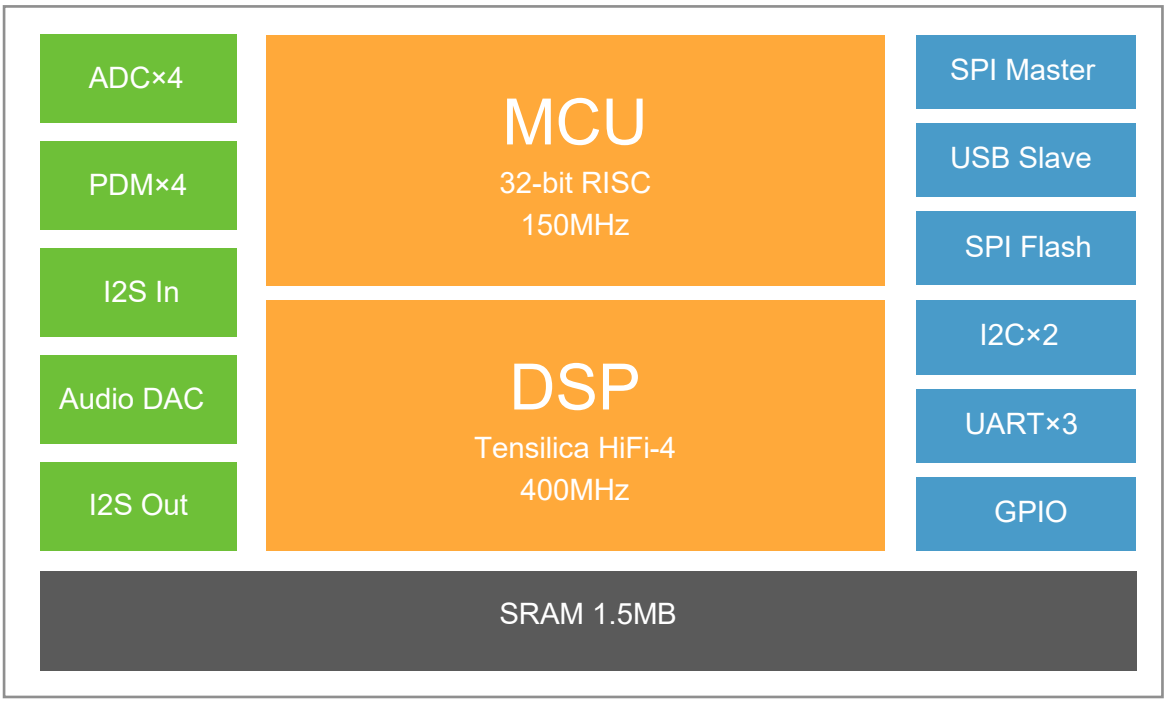


Figure 2- 1 GX8008C chip block diagram

The GX8008C chipset is designed for smart voice front-end system. It has an MCU for system booting, general task management and user applications. A high- performance DSP is built in for smart voice processing like VAD, de-noise, AEC, beamforming, KWS， etc. As front-end chips, GX8008C has various audio interfaces such as ADC, PDM, I2S and USB slave. The chip receives multi-channel microphone signals, and then does signal process and keywords spotting, and after that the data will be transferred to host system by USB slave or other interfaces.

3. Feature List

- **DSP**:
- Cadence Tensilica HIFI-4 voice and audio DSP, frequency up to 400MHz
    - Quad 32-bit MAC, eight 16-bit MAC
    - 32KB Instruction Cache, 32KB Data Cache
    - 64KB DTCM, 64KB PTCM
    - Supports vector float point engine
- **MCU**:
    - 32-bit RISC MCU , frequency up to 150MHz
- **Memory**:
    - Integrates 1.5Mbyte SRAM
    - Supports SPI Nor Flash, maximum speed at 100Mhz.
    - Supports flash XIP access mode
    - Supports standard SPI and quad SPI
- **Analog Mic Input:**
    - Integrates 24-bit 4 channel Sigma-Delta ADC
    - Sample rate: 8KHz, 16KHz, 48KHz
    - Integrates 50dB PGA amplifier for each channel, 2dB per step
    - SNR: 93dB
- **Digital Mic Input:**
    - Supports maximum 4 channel digital mic signal input
    - Supports I2S and PDM
- **Audio Output:**
    - Dual channel 16-bit DAC with up to 93dB SNR
    - I2S master output

- USB 2.0 high or full speed slave mode, support Linux UAC（USB Audio Class）

- **Voice active detection:**
  - Integrates hardware VAD module
  - Supports low-power standby mode with only VAD module on, with power consumption as low as 25mW
- **Interfaces:**
  - Integrates SPI Master
  - Integrates I2C Master and slave
  - 19 GPIOs
  - 8 PWMs
  - UART supports flow control, maximum speed of 3Mbit/s

4. Pin Map

4.1. Acronyms

DP => Digital Power

DG => Digital Ground

AP => Analog Power

AG => Analog Ground

AI => Analog Input

AO => Analog Output

I => Digital Input

O => Digital Output

IO => Digital Bi-directional

AB => Analog Bi-directional

4.2. Pin Map

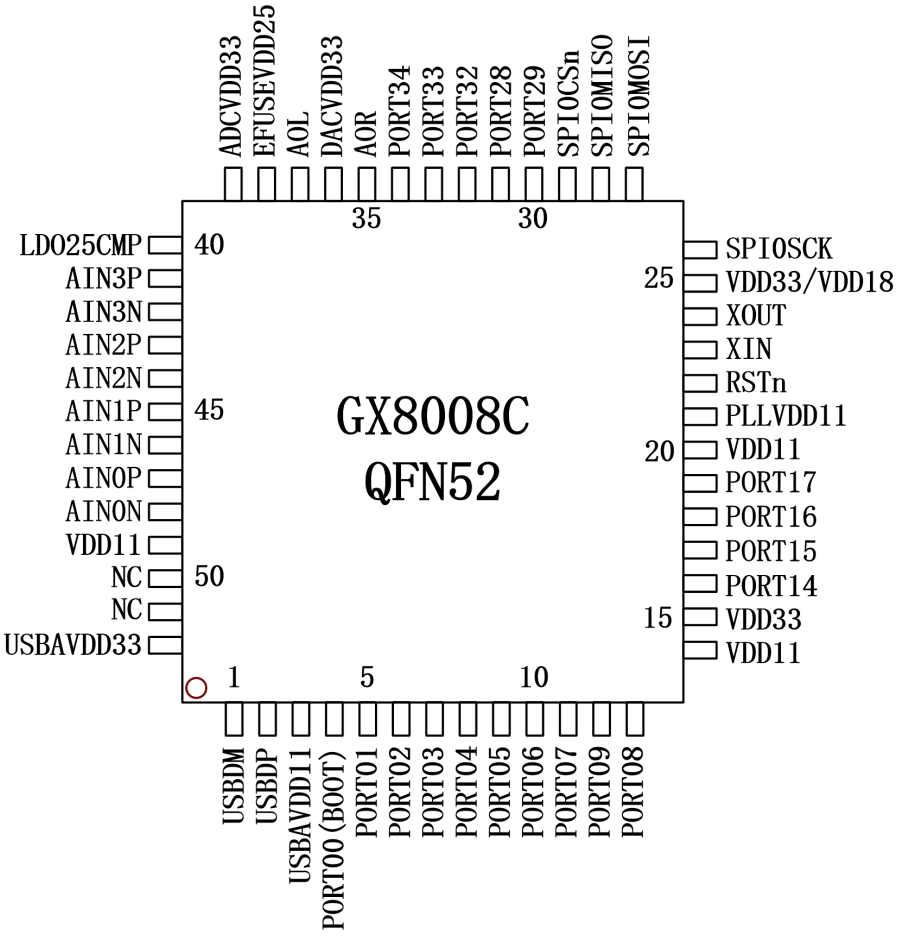


Figure 4- 1 GX8008C pin map

4.2.1. Pin Mux

Table 4-1 GX8008C pin mux

PORTNAME	PULL	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3	FUNCTION4
PORT00	UP	GPIO0				
PORT01	UP	UART1_RX	GPIO1			
PORT02	UP	UART0_RX	GPIO2			
PORT03		UART0_TX	GPIO3			
PORT04		UART1_TX		GPIO4		
PORT05	UP	SDBGTDI	DDBGTDI	UART0_RTS	SDA0	GPIO5
PORT06	UP	SDBGTDO	DDBGTDO	UART0_CTS	SCL0	GPIO6
PORT07	UP	SDBGTMS	DDBGTMS	SDA1	PCM1INBCLK	GPIO7
PORT08	UP	SDBGTCK	DDBGTCK	SDA1	PCM1INLRCK	GPIO8
PORT09	UP	SDBGTRST	DDBGTRST	SCL1	PCM1INDAT0	GPIO9
PORT14	UP	PCMOUTMCLK	DUART_TX	SDA0	SPI1SCK	GPIO14
PORT15	UP	PCMOUTDAT0	SPI1MOSI	SCL0	GPIO15	
PORT16	UP	PCMOUTLRCK	SPI1CSn	GPIO16		
PORT17		PCMOUTBCLK	SPI1MISO	GPIO17		
PORT28	UP	SPI0WP	SDA1	GPIO28		
PORT29	UP	SPI0HOLD	SCL1	GPIO29		
PORT32		PCM0INMCLK	PDMDAT1	GPIO32		
PORT33		PCM0INLRCK	PDMDAT0	PCM0OUTLRCK	GPIO33	
PORT34		PCM0INBCLK	PDMCLK	PCM0OUTBCLK	GPIO34	

4.2.2. Power and Ground Pins

Table 4-2 GX8008C power and ground pins

Pin Number	Pin Name	Type	Description
15,25	VDD33/18	DP	3.3V/1.8V digital power for IO
14,20,49	VDD11	DP	1.1V digital power for core
21	PLLVDD	DP	1.1V digital power for PLL
36	DACVDD33	AP	Power (3.3V) for Audio DAC
38	EFUSE25	AP	Power (2.5V) for EFUSE
39	ADCVDD33	AP	Power (3.3V) for Audio ADC
40	LDO25CMP	AP	Power (2.5V) for ADC power compensate
52	USBVDD33	AP	Power (3.3V) for USB Slave

Pin Number	Pin Name	Type	Description
3	USBVDD11	AP	Power (1.1V) for USB Slave

4.2.3. System Operation Pins

Table 4-3 GX8008C system operation pins

Pin Number	Pin Name	Type	Description
23	XIN	I	Clock input or crystal input
24	XOUT	O	Output for crystal connection
22	RSTn	I	System reset, active low

4.2.4. ADC Interface Pins

Table 4-4 GX8008C ADC interface pins

Pin Number	Pin Name	Type	Description
47	ADCIN0_P	AI	Differential Voltage Inputs, Channel 0
48	ADCIN0_N	AI	Differential Voltage Inputs, Channel 0
45	ADCIN1_P	AI	Differential Voltage Inputs, Channel 1
46	ADCIN1_N	AI	Differential Voltage Inputs, Channel 1
43	ADCIN2_P	AI	Differential Voltage Inputs, Channel 2
44	ADCIN2_N	AI	Differential Voltage Inputs, Channel 2
41	ADCIN3_P	AI	Differential Voltage Inputs, Channel 3
42	ADCIN3_N	AI	Differential Voltage Inputs, Channel 3

4.2.5. SPI Flash Pins

Table 4-5 GX8008C flash pins

Pin Number	Pin Name	Type	Description
26	SPI0SCK	O	SCK of SPI interface
27	SPI0MOSI	O	MOSI of SPI interface
29	SPI0CSn	O	CS of SPI interface
28	SPI0MISO	I	MISO of SPI interface
31	SPI0WP	IO	0: WP of SPI interface
	SDA1	IO	1: Data of I2C 1

Pin Number	Pin Name	Type	Description
	PORT28	IO	2: GPIO 28
30	SPI0HOLD	IO	0: HOLD of SPI interface
	SCL1	IO	1: Clock of I2C 1
	PORT29	IO	2: GPIO 29

4.2.6. Audio Play Interface Pins

Table 4-6 GX8008C audio play interface pins

Pin Number	Pin Name	Type	Description
35	AOR	AO	Audio DAC right channel output
37	AOL	AO	Audio DAC left channel output
16	PCMOUTMCLK	O	0: mclk of audio out i2s interface
	DUARTTX	O	1: DSP UART data transmit
	SDA0	IO	2: Data of I2C 0
	SPI1SCK	O	3: SCK of SPI interface 1
	PORT14	IO	4: GPIO 14
17	PCMOUTDAT	O	0: data of audio out i2s interface
	SPI1MOSI	O	1: MOSI of SPI interface 1
	SCL0	IO	2: Clock of I2C 0
	PORT15	IO	3: GPIO 15
18	PCMOUTLRCK	O	0: lrck of audio out i2s interface
	SPI1CSn	O	1: CS of SPI interface 1
	PORT16	IO	2: GPIO 16
19	PCMOUTBCLK	O	0: bclk of audio out i2s interface
	SPI1MISO	I	1: MISO of SPI interface 1
	PORT17	IO	2: GPIO 17

4.2.7. Communication Interface Pins

Table 4-7 GX8008C communication interface pins

Pin Number	Pin Name	Type	Description
8	UART1TX	O	0: UART1 data transmit

Pin Number	Pin Name	Type	Description
	PORT04	IO	1: GPIO 04
7	UART0TX	O	0: UART0 data transmit
	PORT03	IO	1: Domain1 GPIO 03
6	UART0RX	I	0: UART0 data receive
	PORT02	IO	1: GPIO 02
5	UART1RX	I	0: UART1 data receive
	PORT01	IO	1: GPIO 01
4	BOOT	I	0: a judging condition when starting up from USB
	PORT00	IO	1: GPIO 00

4.2.8. Audio In Interface Pins

Table 4- 8 GX8008C audio in interface pins

Pin Number	Pin Name	Type	Description
32	PCM0INMCLK	I	0: mclk of echo interface
	PDMDAT1	I	1: data1 of audio in pdm interface
	PORT32	IO	2: GPIO 32
33	PCM0INLRCK	I	0: lrck of echo interface
	PDMDAT0	O	1: data0 of audio in pdm interface
	PCM0OUTLRCK	O	2: lrck of audio out i2s interface from core
	PORT33	IO	3: GPIO 33
34	PCM0INBCLK	I	0: bclk of echo interface
	PDMCLK	O	1: mclk of audio in pdm interface
	PCM0OUTBCLK	O	2: bclk of audio out i2s interface from core
	PORT34	IO	3: GPIO 34

4.2.9. USB Interface Pins

Table 4- 9 GX8008C USB interface pins

Pin Number	Pin Name	Type	Description
2	USBDP	AB	USB Slave Data pin Data+
1	USBDM	AB	USB Slave Data pin Data-

4.2.10. JTAG Interface Pins

Table 4- 10 GX8008C JTAG interface pins

Pin number	Pin Name	Type	Description
9	SDBGTDI	I	0: MCU Debug interface data input
	DDBGTDI	I	1: DSP Debug interface data input
	UART0RTS	IO	2: UART0 Require To Send
	SDA0	IO	3: Data of I2C 0
	PORT05	IO	4: GPIO 05
10	SDBGTDO	O	0: MCU Debug interface data output
	DDBGTDO	O	1: DSP Debug interface data output
	UART0CTS	IO	2: UART0 Clear To Send
	SCL0	IO	3: Clock of I2C 0
	PORT06	IO	4: GPIO 06
11	SDBGTMS	I	0: MCU Debug interface mode select
	DDBGTMS	I	1: DSP Debug interface mode select
	SDA1	IO	2: Data of I2C 1
	PCM1INBCLK	I	3: bclk of echo interface
	PORT07	IO	4: GPIO 07
12	SDBGTRST	I	0: MCU Debug interface reset
	DDBGTRST	I	1: DSP Debug interface reset
	SCL1	IO	2: Clock of I2C 1
	PCM1INDAT0	I	3: data of echo interface
	PORT09	IO	4: GPIO 09
13	SDBGTCK	I	0: MCU Debug interface clock
	DDBGTCK	I	1: DSP Debug interface clock
	SDA1	IO	2: Data of I2C 1
	PCM1INLRCK	I	3: lrck of echo interface
	PORT08	IO	4: GPIO 08

5. Applications

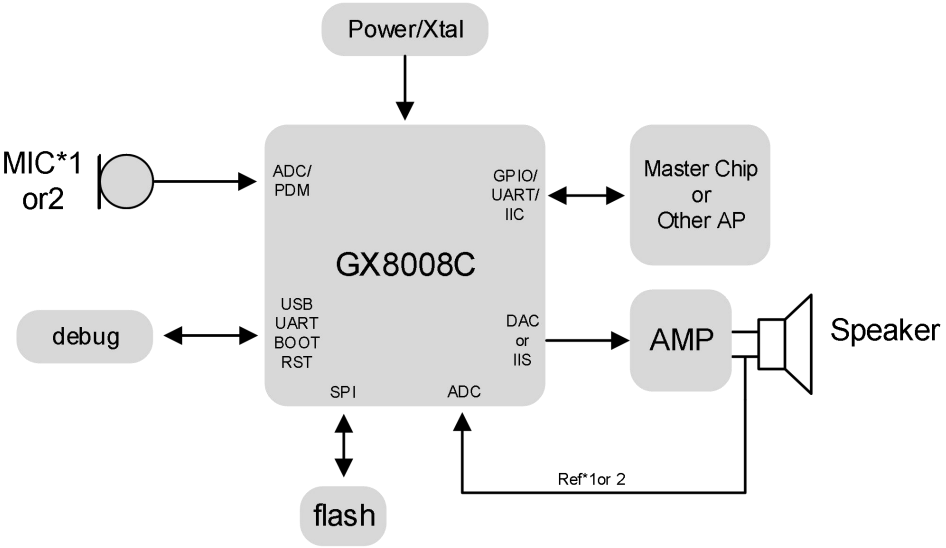


Figure 5- 1 Classic application diagram for smart voice control

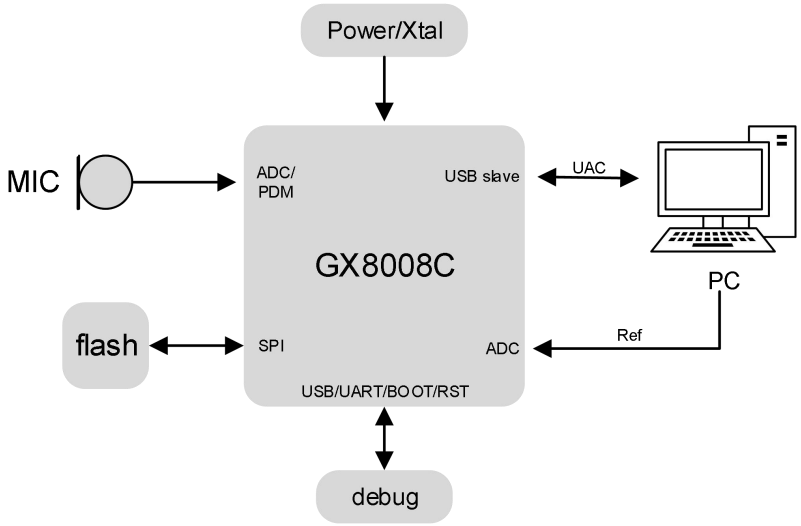


Figure 5- 2 Application diagram for smart USB audio device

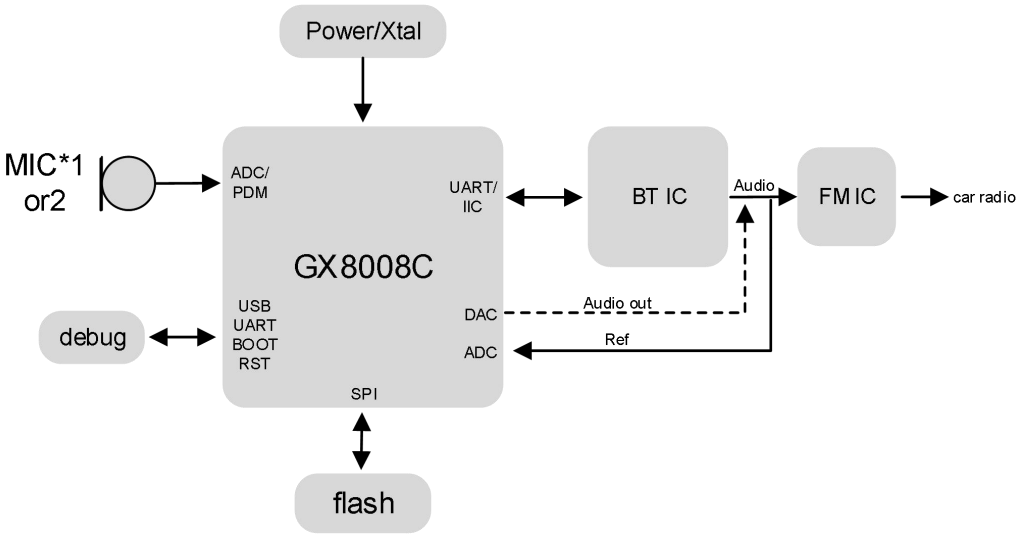


Figure 5- 3 Application diagram for smart voice with Bluetooth and radio in vehicles

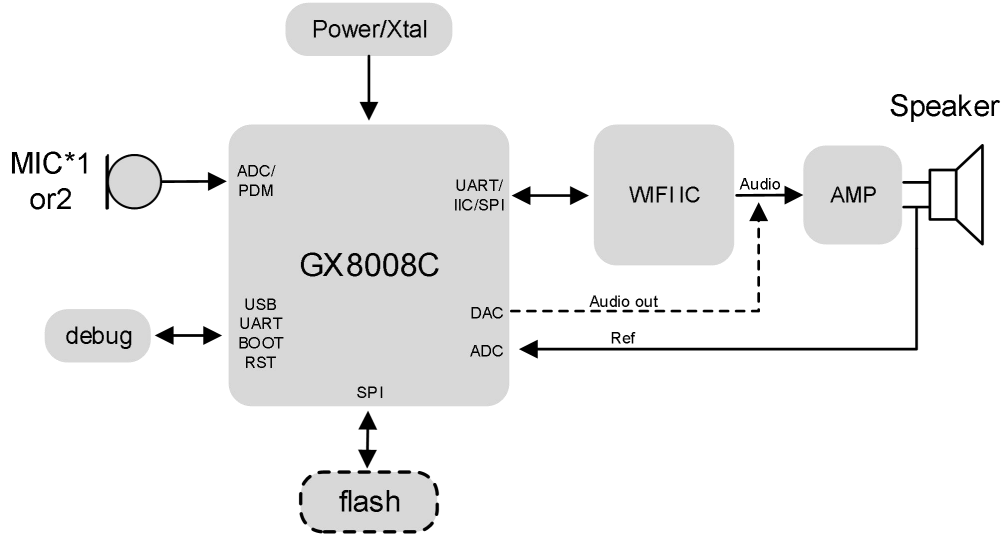


Figure 5- 4 Application diagram for online smart voice control with WiFi

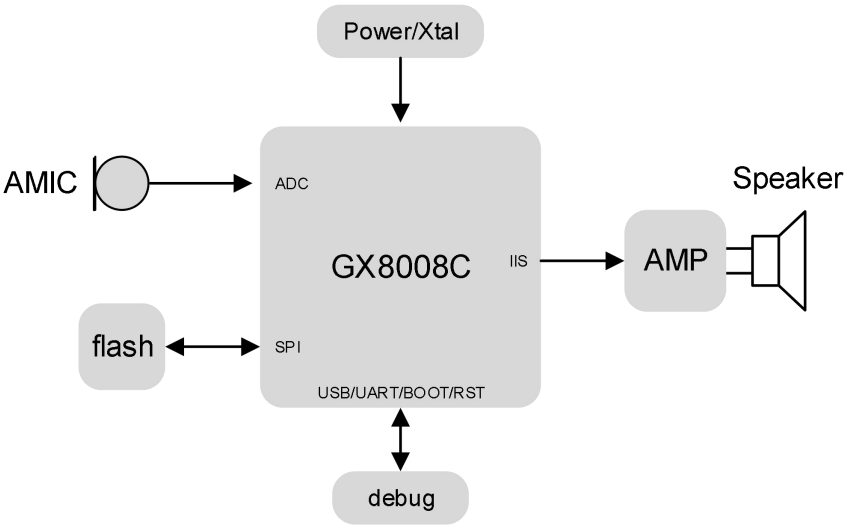


Figure 5- 5 Application diagram for Anti howling microphone

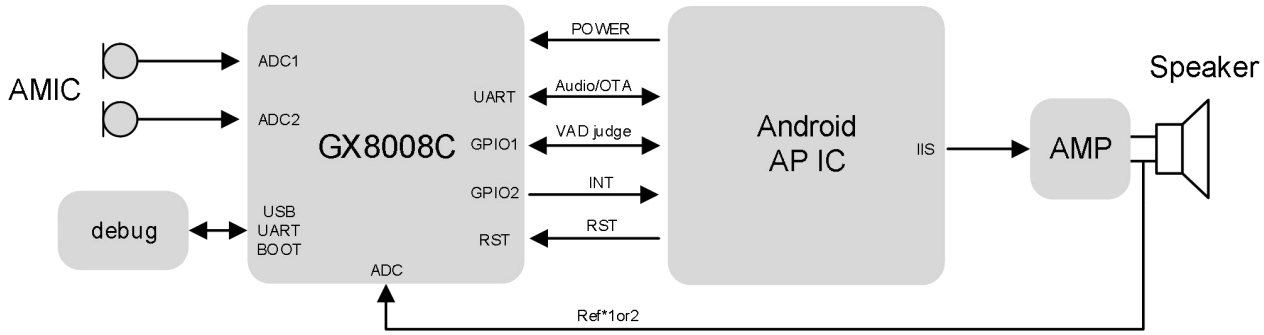


Figure 5- 6 Application diagram of acoustic frontend of Android AP

6. Electronic Specification

6.1. Recommended Operating Condition for 3.3V IO Application

Table 6-1 Recommended operating conditions for 3.3V IO

Parameters	Min	Typ	Max	Units
IO Power Supply Voltage(VDD_IO)	2.97	3.3	3.6	V
Output High Level (VOH)	2.4	2.8	3.6	V
Output Low Level (VOL)	0	0.2	0.4	V
Output Drive Strength	4	4	4	mA
Pull-up Resistor	58	86	133	kΩ
Pull-down Resistor	52	78	128	kΩ
Input High Level (VIH)	2.0	2.8	3.6	V
Input Low Level (VIL)	-0.3	0	0.8	V

6.2. Recommended Operating Condition for 1.8V IO Application

Table 6-2 Recommended operating conditions for 1.8V IO

Parameters	Min	Typ	Max	Units
IO Power Supply Voltage(VDD_IO)	1.62	1.8	1.98	V
Output High Level (VOH)	1.35	1.8	1.98	V
Output Low Level (VOL)	0	0.2	0.45	V
Output Drive Strength	4	4	4	mA
Pull-up Resistor	117	194	331	kΩ
Pull-down Resistor	91	159	291	kΩ
Input High Level (VIH)	1.17	1.8	3.6	V
Input Low Level (VIL)	-0.3	0	0.63	V

6.3. Recommended Operating Condition

Table 6-3 Recommended operating conditions

Parameters	Min	Typ	Max	Units
1.1V Power Supply Voltage	1.05	1.10	1.15	V
1.1V Power Supply Current	20	200	250	mA
2.5V Power Supply Voltage	2.35	2.5	2.65	V
2.5V Power Supply Current	4.5	5	5.5	mA
3.3V IO Application				
3.3V Power Supply Voltage	3.0	3.3	3.45	V
3.3V Power Supply Current		8		mA
1.8V IO Application				
1.8V Power Supply Voltage	1.65	1.8	1.98	V
1.8V Power Supply Current		2		mA
Operating Ambient Temperature	-40	30	85	℃
Thermal Temperature		32		℃
Moisture Sensitivity Level		MSL3		

6.4. Absolute Maximum Ratings

Table 6-4 Absolute maximum ratings

Parameters	Min	Typ	Max	Units
1.1V Supply Voltage	1.05	1.1	1.21	V
3.3V IO Power Supply Voltage(VDD_IO)	3.0	3.3	3.6	V
1.8V IO Power Supply Voltage(VDD_IO)	1.62	1.8	1.98	
LDO 2.5V Supply Voltage	2.25		2.75	V
Transient I/O Voltage	VSS-0.5V		VIO+0.5V	V
Storage Temperature	-40	20	120	℃

6.5. Timing Information

6.5.1. I2C

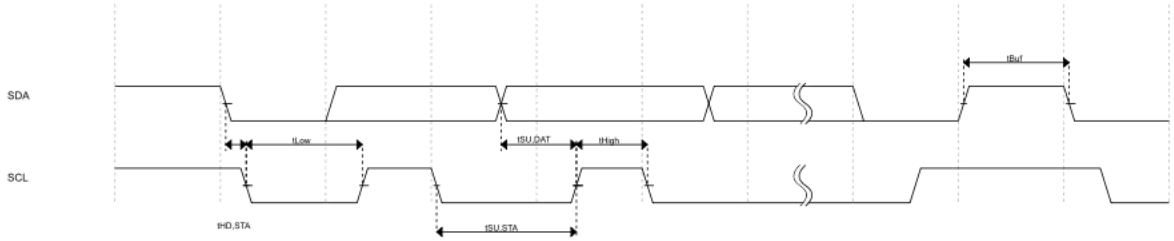


Figure 6- 1 I2C Interface Timing Diagram

Table 6- 5 I2C Interface Timing Specification, SF mode

Parmaeter	Symbol	Standard-mode (min)	Fast-mode (min)	Unit
SCL clock frequency	SCL	100	400	kHz
Hold time START condition	tHD,STA	4.0	0.6	us
Low period of the SCL clock	tLow	4.7	1.3	us
High period of the SCL clock	tHigh	4.0	0.6	us
Bus free time between a STOP and START condition	tBuf	4.7	1.3	us
Data set-up time	tSU;DAT	250	100	us
Setup-up time fo a repeated START condition	tSU;SAT	4.7	00.6	us

6.5.2. I2S

6.5.2.1. 64fs I2S Interfac

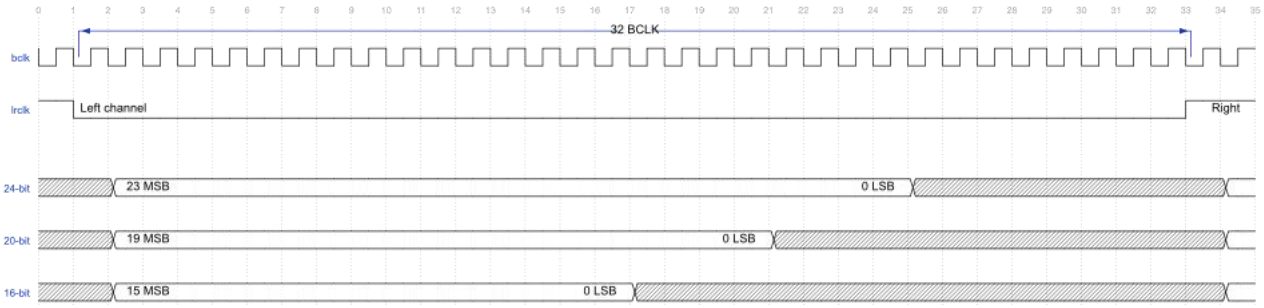


Figure 6- 2 I2S 64fs Interface Timing Diagram

6.5.2.2. I2S Left/Right Interface

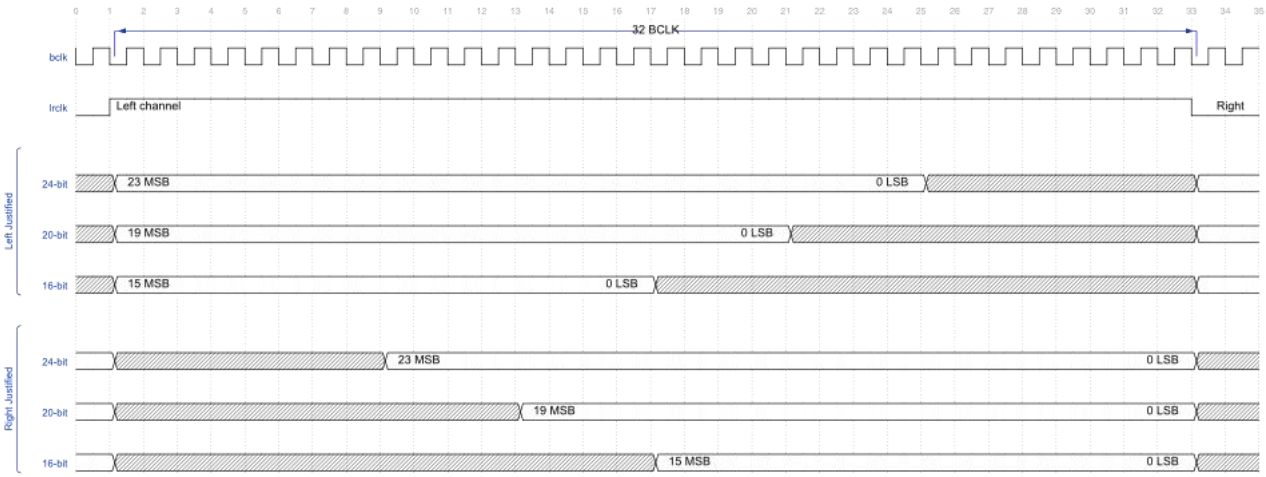


Figure 6- 3 I2S 64fps Left/Right Interface Timing Diagram

Table 6- 6 I2S Timing Specification

Parmaeter	Symbol	Min	Typ	Max	Unit
Master clock	SCL		24.576		MHz
Bit clock	BCLK		3.072		MHz
Left/Right clock	tLow		48		KHz

6.5.3. Flash SPI

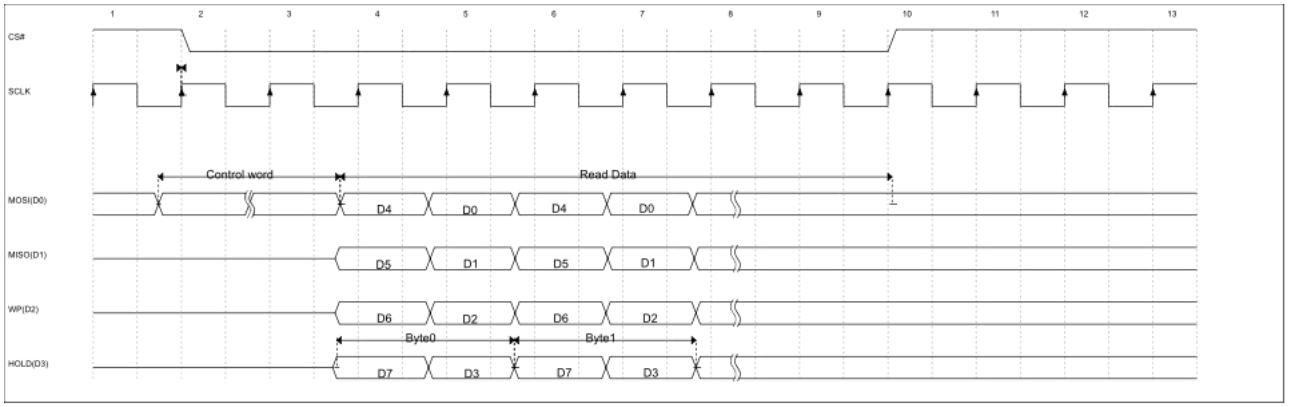


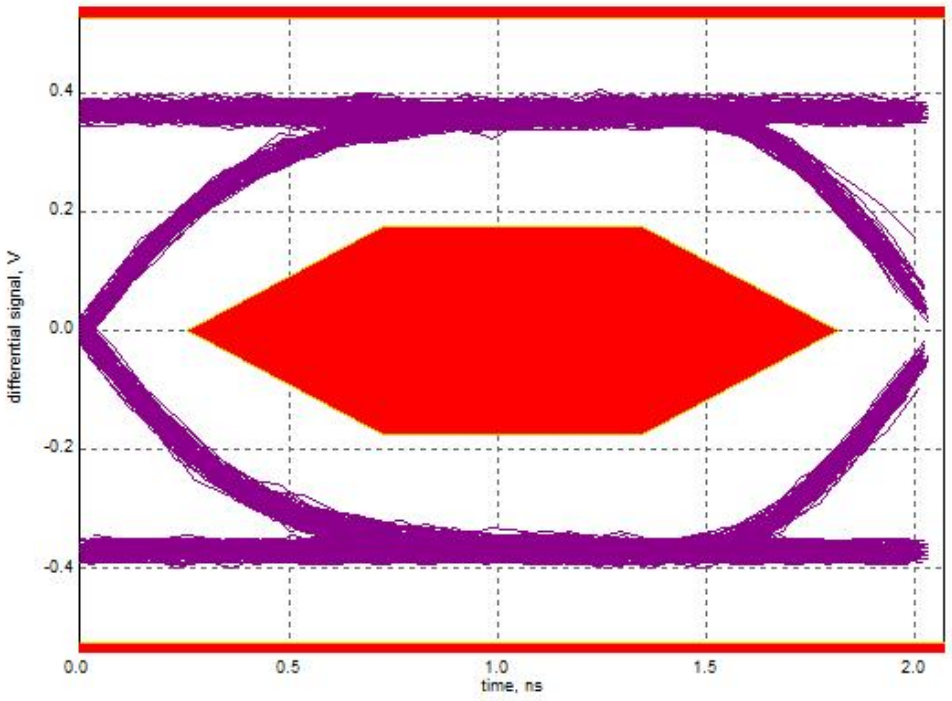
Figure 6- 4 I2S 64fps Left/Right Interface Timing Diagram

Table 6- 7 I2S Timing Specification

Symbol	Parameter	Min	Typ	Max	Unit
Fsclk	SCLK frequency range			75	Mhz

Symbol	Parameter	Min	Typ	Max	Unit
Bytefifo	Fifo			64	Bytes
Tsclk_LO	Clock Low time	1/2 Fsclk(max)			
Tsclk_HI	Clock High time	1/2 Fsclk(max)			

6.5.4. USB eye diagram



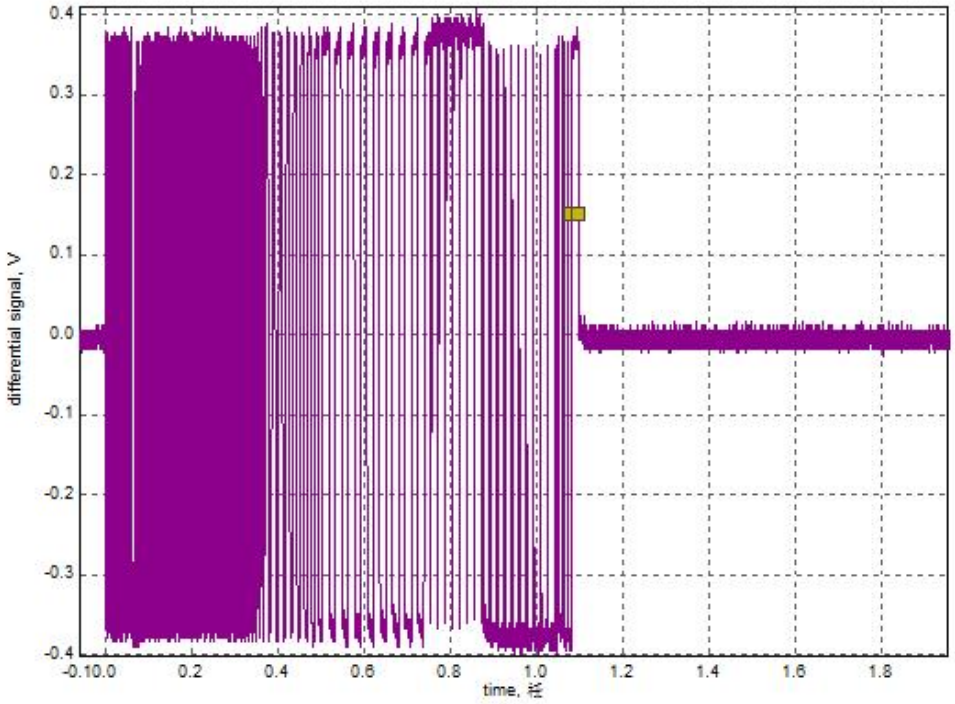


Figure 6-5 USB eye diagram

6.6. ADC Characteristics

Table 6-8 The effect of the clock on SNR

ADC Parameter					
AVDD33=3.3V, AVDD25=2.5V, VDIG=1.1V, ADC_GAIN=0dB					
Parameter	Test condition	Min	Typ	Max	Unit
Input Common Mode			1.25		V
common mode bias			25/250		KΩ
boost_gain			0/16/30		dB
pga_gain			0~20		dB
Full Scale input Voltage	(THD+N=-40dB)		1.7		Vrms
Noise	Fs=16KHz A-weighted		-93		dBFS
SNR	Fs=16KHz A-weighted		93.2		dBFS
Dynamic Range	1.7mVrms input (-60dB of max input level) Fs=16KHz A-weighted		93		dB
THD+N	Best at 707mVrms input (ADC_GAIN=2dB) Fs=16KHz A-weighted		-70.1		dB

Table 6-9 Effect of PGA on SNR

boost_gain	pga_gain	total_gain	chopper	SNR(dB)
0	0	0	-	93.24
0	2	2	-	92.99
0	4	4	-	92.85
0	6	6	-	92.65
0	8	8	-	92.38
0	10	10	-	91.85
0	12	12	-	91.35
0	14	14	-	90.53
0	16	16	-	89.64
16	2	18	CLK/16	90.84
16	4	20	CLK/16	89.42
16	6	22	CLK/16	87.92
16	8	24	CLK/16	86.33
16	10	26	CLK/16	84.73
16	12	28	CLK/16	82.97
16	14	30	CLK/16	81.14
30	2	32	CLK/32	85.63
30	4	34	CLK/32	83.87
30	6	36	CLK/32	81.96
30	8	38	CLK/32	80.09
30	10	40	CLK/32	78.18
30	12	42	CLK/32	76.24
30	14	44	CLK/32	74.31
30	16	46	CLK/32	72.32
30	18	48	CLK/32	70.30
30	20	50	CLK/32	68.35

6.7. Audio LDO Characteristics

Table 6-5 LDO parameter

Audio LDO parameter				
IO Parameters	Min	Typ	Max	Unit
Analog Power Supply Voltage(3.3V)	3	3.3	3.6	V
Analog Power Voltage Outpu(2.5V)	2.25	2.5	2.75	V
Input Impedance		12.5		KΩ
PSRR		-90		dB
Input Voltage(Vp-p)		2.4		V

6.8. DAC Characteristics

Table 6- 5 External 2x op amp zoom

Test Items	Left and right channel	Test Values	Remark 1	Remark 2
RMS Level	L	6.20dBu	1.585Vrms	
	R	6.17dBu	1.577Vrms	
THD	L	0.0085%		A-wt
	R	0.0066%		
THD+N	L	0.0085%		A-wt
	R	0.0070%		
Cross Talk	L->R	-85.5dBu	impedance 200K	A-wt
	R->L	-80.6dBu		
SNR	L	-93.21dBu	impedance 200K	A-wt
	R	-93.12dBu		
Sample Freq	8K(min)		48K(max)	Hz

6.9. Power on and Reset

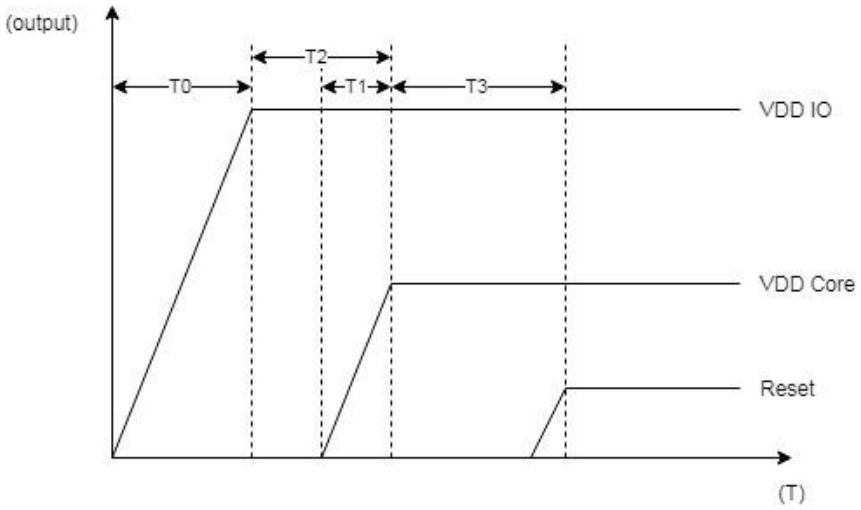


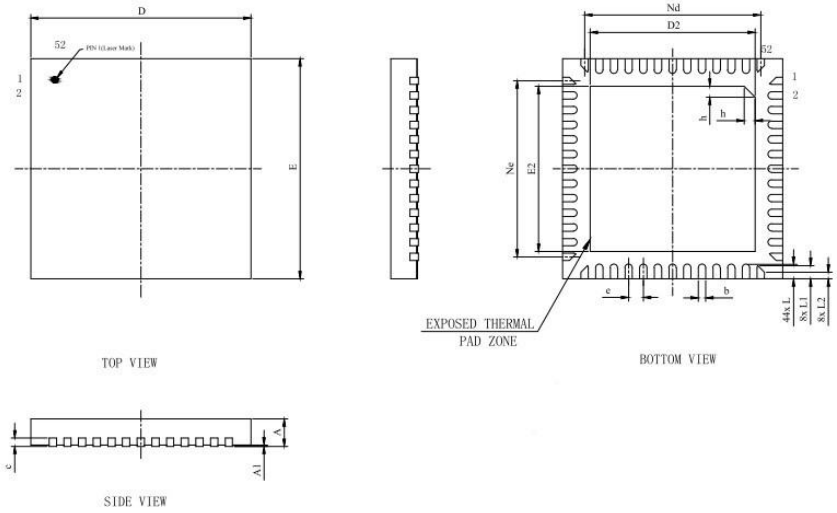
Figure 6-6 IO,CORE&RESET time map

Table 6-6 Power on and Reset time parameter

Parameter	Description	MIN	MAX	Unit
T0	IO power rise up time	0	3	ms
T1	Core power rise up time	0	3	ms
T2	Core power rise up delay time compare with IO power	0	3	ms
T3	Reset delay time	40		ms

7. Package Information

7.1. Package Specification



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.035	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.40	4.50	4.60
e	0.40BSC		
Nd	4.80BSC		
E	5.90	6.00	6.10
E2	4.40	4.50	4.60
Ne	4.80BSC		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F载体尺寸 (mil)	185*185		

Figure 7- 1 QFN52 package specification

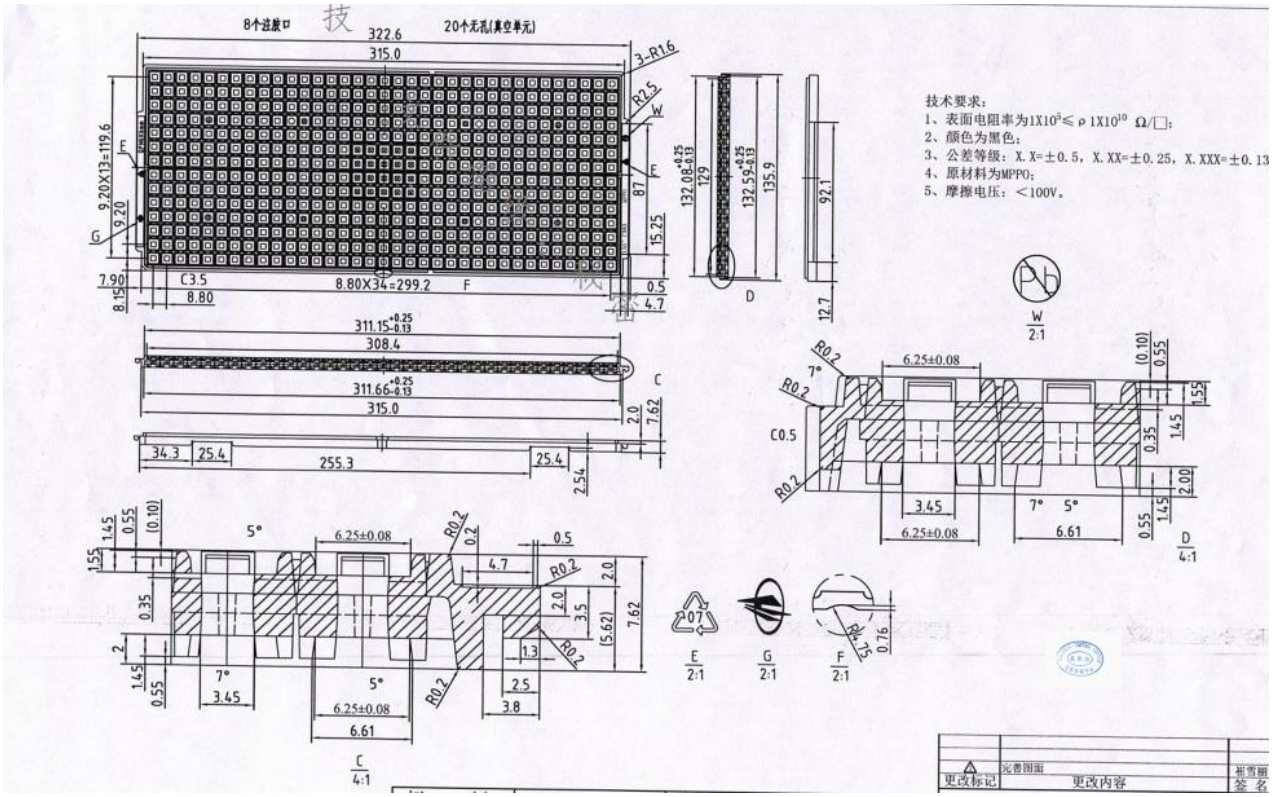


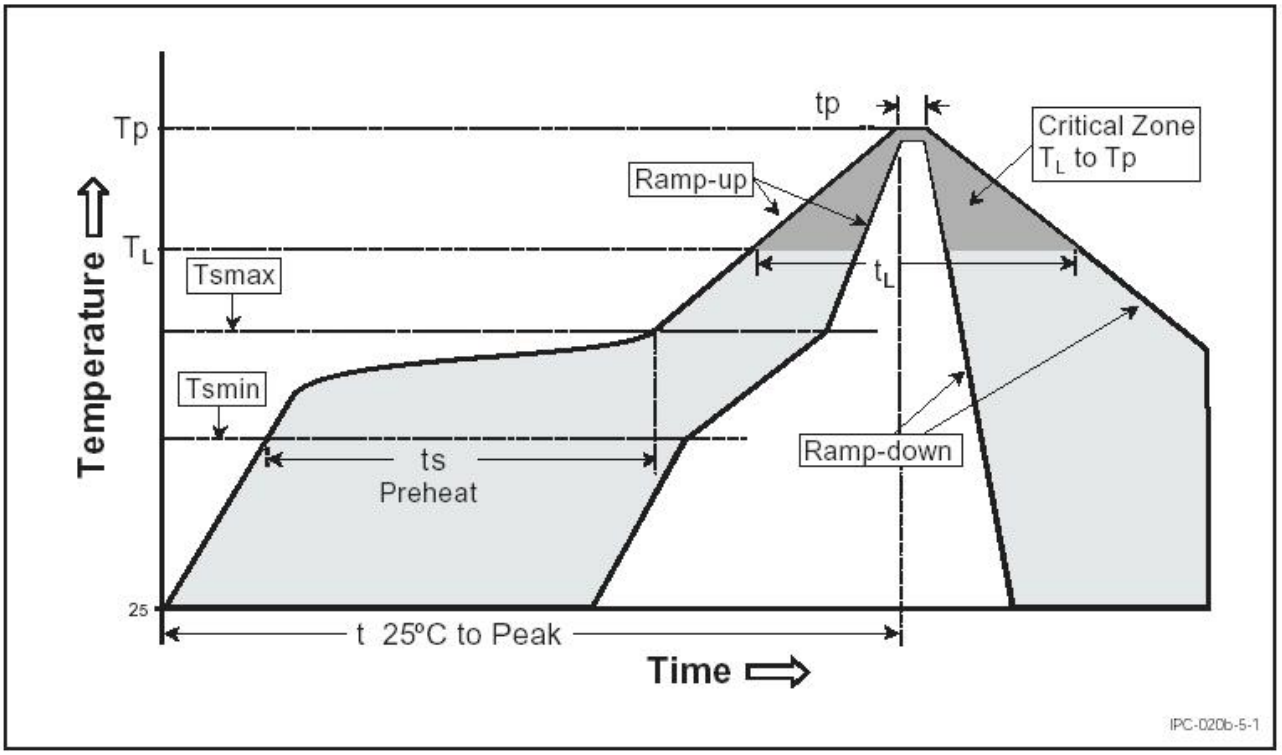
Figure 7- 2 QFN52 Chip Tray specification

7.2. Convection Reflow Profile

Table 7-1 Convection reflow profile

Profile Feature	Note	Pb-Free Assembly
Average ramp-up rate	Tsmax to Tp	0.6~1.5℃/sec
Preheat	-Temperature Min (Tsmin)	150℃
	-Temperature Max(Tsmax)	200℃
	-Time(min to max)(ts)	60-180sec
Time maintained above:	-Temperature (TL)	217℃
	-Time (tL)	60-150 sec
Peak Temperature (Tp)		245±5℃
Time within 5℃ of actual Peak Temperature (tp)		≤30sec
Ramp-down Rate		≤3℃/ sec
Time 25℃ to Peak Temperature		≤8 min

Figure 7-3 Convection Reflow Profile



Note:

- All temperatures refer to topside of the package, measured on the package body surface.
- Actual board assembly depends on other parts on board density and follow solder paste manufacturers' guideline.

8. Ordering Information

Table 8- 1 Ordering information

Ordering Code	Description	Package
GX8008C	OTP Area read only	QFN52
GX8008C-X	OTP Area open to customer to read and write	QFN52

Revision History:

Version	Time	Change Log	Author
V1.0	2019.09.24	Initial version	Jing Lin
V1.1	2020.02.28	Fixed application figure and adjusted format	Hudong Chen, Jing Lin
V1.2	2021.01.21	Fixed pin map pull up	Chenshu
V1.3	2021.11.18	Add 8008c-x description and fix some ADC/DAC description.	Lingyun
V1.4	2021.12.6	I-TCM and D-TCM size 64KB	Lingyun
V1.5	2022.6.9	Add Power on and reset description,fix the Operating Ambient Temperature	Weidong
V2.0	2023.8.18	Add 1.8V IO application and convection reflow profile	Chenshu

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