GX8010

A Neural Processor for AI & IoT

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1. General Introduction

GX8010 is an embedded SoC chip designed for Artificial Intelligence (AI) and Internet of Things (IoT) applications. Targeting at the features of AI applications, GX8010 is uniquely designed in a heterogeneous multi-core architecture, which integrates self-developed Neural Process Unit (NPU), DSP for voice processing, ARM Cortex A7 CPU, Audio decoder and other modules. It enables the product to perform deep neural network computation and process microphone array signals offline. In addition, considering the requirement of low power consumption, GX8010 is specifically assigned to support multi-level low power control, making it possible to be voice woken up even in the ultra low-power standby state. The high degree of integration of GX8010, which includes ADC, audio codec, rich peripheral interfaces as well as an embedded 128Mbyte DRAM, makes its size smaller, power consumption lower, and the entire hardware design simpler.

The highlights of the chip includes following features:

- **NPU**: neural process unit that enables chipset to run deep learning model locally
- **sNPU**: second NPU dedicated for the model of key words spotting.
- **CPU**: ARM Cortex A7 1GHz with FPU and Neon DSP，with 32k/32k L1 cache, and 128KB L2 cache
- **DSP**: Tensilica HIFI4 DSP processor, speed up to 400MHz
- **Mic Array**: supports 8 analog or digital mic, both PDM and I2S
- **Camera**: supports BT1120 and USB interfaces, with graphic accelerator integrated
- **Audio**: supports mainstream audio format decoding and direct DAC output
- **Video**: hardware JPEG decoder and encoder
- **Security**: integrates OTP, and AES / 3DES / DES engine, and supports security boot and content protection.
- **Peripherals**: SPI master/Slave, SDIO master, I2C, UART, PWM, USB Slave/Master
- **Package**: TFBGA208, 12x12mm

2. Chip Architecture

2.1. Block Diagram

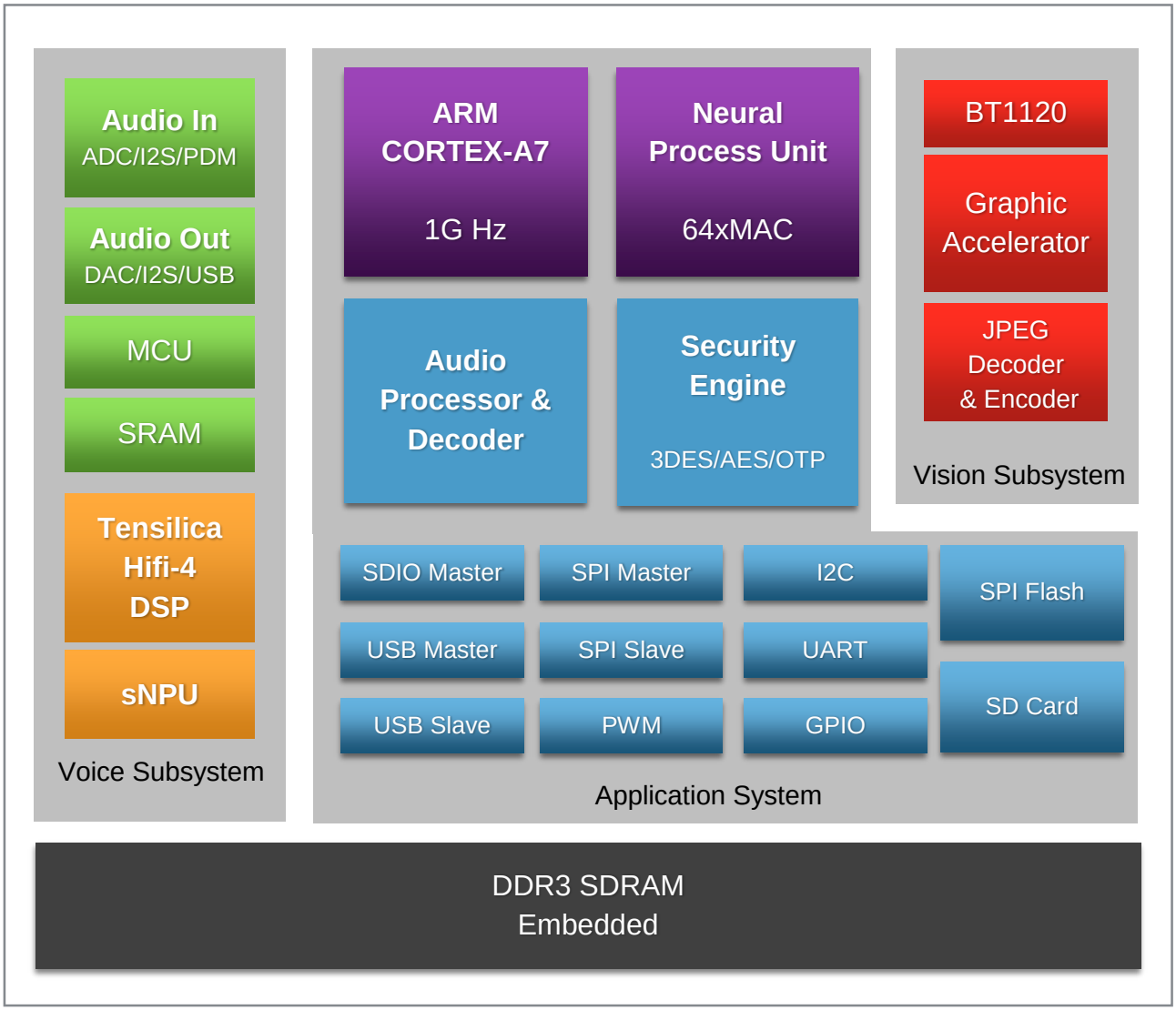


Figure 2-1 GX8010 Chip Block Diagram

The GX8010 chipset can be divided into four part: the first part is voice subsystem which process the multi-channel microphone signal and detect the wake-up keywords, the second part is vision subsystem which receive camera data and do related processing, the third part is application system which run the OS and the application frameworks, the last one is a SIP packaged DDR3 SDRAM which has 128M or 256M bytes memory size.

2.2. Power Domain Specification

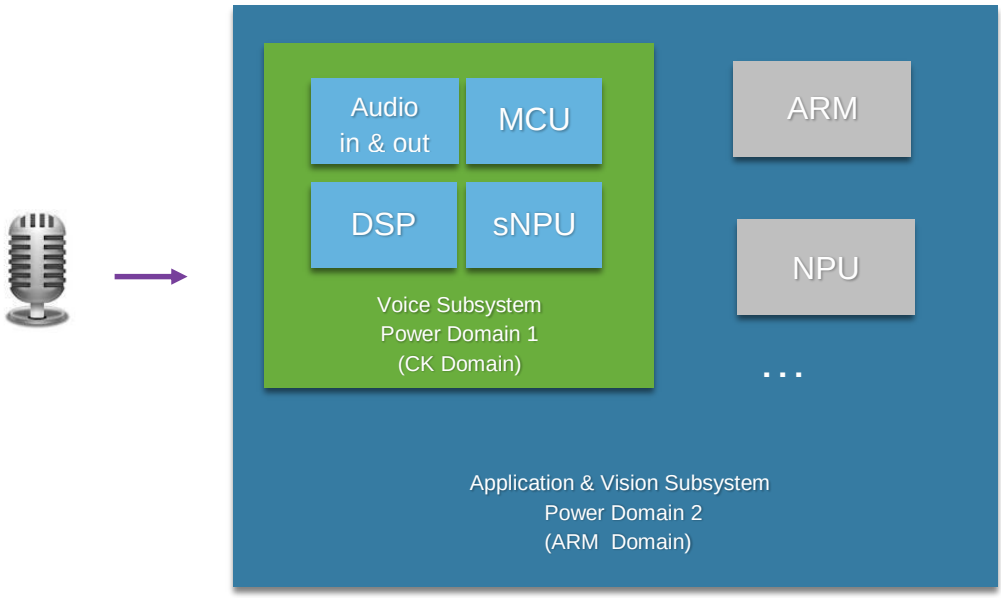


Figure 2-1 GX8010 Chip Power Domain

The GX8010 chipset internally splits into two power domain. The power domain 1 is always on and includes the modules in Voice subsystem. The modules in Application subsystem and Vision subsystem are in power domain 2. When in low-power standby mode, system can turn off the power domain 2, and power domain 1 keeps working to detect the voice command. Once the wake-up keywords were detected, the system will turn on the power domain 2.

3. Feature list

3.1. Voice Subsystem

- **DSP:**
    - Cadence Tensilica HIFI4 voice and audio DSP, frequency up to 400MHz
    - Quad 32-bit MAC, eight 16-bit MAC
    - 32KB Instruction Cache, 32KB Data Cache
    - 32KB DTCM, 32KB PTCM
    - Support JTAG
- **sNPU:**
    - Neural process unit dedicated for keywords spotting
    - 32 MAC, support DNN/CNN/LSTM and other classic models.
- **MCU:**
    - 32bit RISC MCU, frequency up to 150MHz
    - System booting and low power standby control
    - Coordinate the work flow of DSP, sNPU and the main CPU
- **Digital Mic Input:**
    - Support maximum 8 channel digital mic signal input
    - Support I2S and PDM
- **Analog Mic Input:**
    - Integrate 16-bit 8 channel Sigma-Delta ADC
    - Sample rate: 8KHz, 16KHz, 48KHz
    - Integrate PGA amplifier for each channel, 2dB per step
    - SNR: 85dB
- **Audio Output:**
    - Dual channel 16-bit DAC with up to 95dB SNR
    - SPDIF and I2S output
    - USB 2.0 full speed slave mode, support USB audio class

3.2. Vision Subsystem

- **Camera**

- Support BT1120 & USB input
- 16 / 8 bit, resolution up to 1920x1080p
- Output simultaneously original and compressed pictures
- Support format conversion and window clip

- **Graphic Accelerator**
  - Integrate graphic accelerator for various graphic process.
- **JPEG Encoder:**
  - JPEG encoding hardware accelerator supports Baseline.
  - Up to 8K*8K JPEG encoding
  - MJPEG encoding up to 1080p@30fps
- **JPEG Decoder:**
  - JPEG hardware accelerator supporting Baseline and Progressive mode.
  - Up to 8K*8K JPEG decoding
  - Support MJPEG decoding

3.3. Application System

- **NPU (Neural Process Unit)**
  - Neural Process Unit, enable the chipset to run neural models locally
  - 64 MAC array
  - Support float32 and float16 data format
  - Support DNN/CNN/LSTM and other classic deep learning models.
  - Support activation function such as Sigmoid, Tanh, Relu, Soft plus
  - Support neural network weights compression
  - Tensorflow compatible
- **CPU**
  - ARM Cortex A7 up to 1GHz
  - 32KB L1 instruction cache, 32KB L1 data cache, and 128KB L2 cache
  - Integrate FPU and Neon DSP
  - Support dynamic frequency adjustment
- **Memory**

- Support SPI Nor and Nand Flash, maximum size up to 256MB
- Support SD card
- Embbed 1Gb DDR3 up to 600MHz

- **Audio Processor and Decoder:**
  - MPEG1 I/II, Layer I/II, MP3 decoding
  - MPEG-4 AAC and AAC plus (HE-AAC v1 and v2) decoding
  - 3 channel audio mixing
  - Audio sample rate conversion
- **Communication System**
  - I2Cx2
  - USB 2.0 high speed host interface for external devices
  - USB 2.0 high speed slave interface for UAC、HID and debug port
  - General purpose DMA
  - General purpose SDIO/SPI Master
  - SPI slave
  - Timerx4
  - SD card controllerx1
  - UARTx4
  - PWM controller
  - GPIO
- **Security Engine**
  - Integrate OTP
  - Unique ID per chip
  - Integrate AES/DES/3DES engine
  - Support security boot
  - Support content protection for NPU models

4. Pin Map

4.1. Pin Map

	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
01		SPI1CSn_NDBGTMS_ADBGTMS_PD2PORT32	SPI1SCK_NDBGTDI_ADBGTDI_PD2PORT30	UART2RX_SDA2_PD2PORT28		DBGTDO_PD2PORT24	UART3TX_SCL3_PD2PORT22		BTDAT13_PD2PORT18	BTDAT12_PD2PORT17		BTDAT06_PD2PORT11	BTDAT04_PD2PORT09	BTCLK_OUT_PD2PORT08	BTCLK_IN_PD2PORT04
02	SPI2CSn_PD2PORT36	SPI2SCK_NDBGTRST_ADBGTRST_PD2PORT34	SPI1MISO_NDBGTCK_ADBGTCK_PD2PORT33	UART2TX_SCL2_PD2PORT29	DBGTCK_PD2PORT26	DBGTMS_PD2PORT25	UART3RX_SDA3_PD2PORT21	PD2VDD11	BTDAT15_PD2PORT20	BTDAT14_PD2PORT19	BTDAT10_PD2PORT15	BTDAT08_PD2PORT13	BTDAT05_PD2PORT10	BTCLK_VSYNC_PD2PORT06	BTDAT01_PD2PORT01
03		SPI2MOSI_PD2PORT35	SPI2MISO_PD2PORT37	SPI1MOSI_NDBGTDO_ADBGTDO_PD2PORT31	DBGTRST_PD2PORT27	GND	DBGTDI_PD2PORT23	GND		GND	BTDAT11_PD2PORT16	BTDAT09_PD2PORT14	BTDAT07_PD2PORT12_NUARTTX_AUARTTX	BTCLK_HREF_PD2PORT07	BTDAT02_PD2PORT02
04	SD0DAT0_PD2PORT40	SD0DAT1_PD2PORT39	SD0CDn_PD2PORT38	PD2VDD11	GND	VDDP15_DDR	VREF	VDDP15_DDR	PD2VDD11	PD2VDD11	PD2VDD33	PD2BTVDD30	BT_RESET_PD2PORT05	BTDAT03_PD2PORT03	BTDAT00_PD2PORT00
05	SD0CMD_PD2PORT42	SD0DAT3_PD2PORT43	SD0CLK_PD2PORT41	GND	PD2VDD11	PD2VDD11	VDDP15_DDR	PD2VDD11	VDDP15_DDR	GND	VDDP15_DDR	GND	AIN7P	AIN7N	
06		SD0DAT2_PD2PORT44	SD1CDn_PD2PORT45	PD2VDD33	PD2VDD11	GND	PD2VDD11	GND	GND	GND	GND	BIAS7	BIAS6	AIN6P	AIN6N
07	SD1CLK_PD2PORT48	SD1DAT1_PD2PORT46	SD1DAT0_PD2PORT47	GND	PD2VDD11	GND	GND	GND	GND	GND	GND	BIAS5	AIN5P	AIN5N	
08	SD1DAT3_PD2PORT50	SD1CMD_PD2PORT49	SD1DAT2_PD2PORT51	PD2VDD11	GND	GND	GND	GND	GND	GND	GND	GND	BIAS4	AIN4N	AIN4P
09		PD2USBDM	PD2USBDP	PD2USBAVDD33	PD2VDD11	GND	GND	GND	GND	GND	GND	LDO25CMP	BIAS3	AIN3N	
10	PD1USBDP	PD1USBDM	GND	PD2USBAVDD11	GND	GND	GND	GND	GND	GND	GND	EFUSEVDD25	BIAS2	AIN3P	AIN2N
11		UART0RX_PD1PORT02	UART0TX_PD1PORT03	PD1USBAVDD33	PD1VDD11	PD1VDD11	GND	GND	GND	GND	GND	AADCVDD33	BIAS1	AIN2P	
12	OTP_AVDD_ENV_PD1PORT04	PD1PORT00(boot)	POWER_DOWN_PD1PORT01	PD1USBAVDD11	PD1VDD11	PD1VDD33	PD1VDD11	PD1VDD11	PD1VDD11	PD1VDD33	GND	ADACVDD33	BIAS0	AIN1P	AIN1N
13	SDBGTDO_PD1PORT06	SDBGTDI_PD1PORT05	SDBGTMS_PD1PORT07	PCM0UTMCLK_DUARTTX_SNUARTTX_PD1PORT14	UART1RX_PD1PORT18	DDBGTDO_SNDBGTDO_PD1PORT21	DDBGTRST_SNDBGTRST_PD1PORT24	DUARTTX_SNUARTTX_PD1PORT25	RSTn	SPI0MOSI	SDA0_PD1PORT26	SDA1_PD1PORT28	PCM0INLRCK_PDMDAT0_PCM0OUTLRCK_PD1PORT33	AIN0P	AIN0N
14	SDBGTCK_PD1PORT08	SDBGTRST_PD1PORT09	PCM1INDAT0_PD1PORT13	PCM0UTLRCK_PD1PORT16	UART1TX_PD1PORT19	DDBGTDI_SNDBGTDI_PD1PORT20	DDBGTCK_SNDBGTCK_PD1PORT23	XOUT	SPI0SCK	SPI0MISO	SCL0_PD1PORT27	SCL1_PD1PORT29	PCM0INDAT0_PDMDAT2_PD1PORT31	IR_PD1PORT35	AOL
15	PCM1INLRCK_PD1PORT12	PCM1INBCLK_PD1PORT11	PCM0UTDAT0_SPDIF_PD1PORT15	PCM0UTBCLK_PD1PORT17		DDBGTMS_SNDBGTMS_PD1PORT22		XIN		SPI0CSn		PCM0INDAT1_PDMDAT3_PD1PORT30	PCM0INMCLK_PDMDAT1_PD1PORT32	PCM0INBCLK_PDMCLK_PCM0OUTBCLK_PD1PORT34	AOR

Figure 4-1 GX8010 Pin Map

4.2. Acronyms

DP => Digital Power
AP => Analog Power
AI => Analog Input
I => Digital Input
IO => Digital Bi-directional

DG => Digital Ground
AG => Analog Ground
AO => Analog Output
O => Digital Output
AB => Analog Bi-directional

4.3. Pin Mux

Table 4-1 Pin Mux

Domain	PORT_NAME	PULL	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3	FUNCTION4	FUNCTION5
CK Domain	PD1PORT00	UP	GPIO0					
CK Domain	PD1PORT01		POWER_DOWN	GPIO1				
CK Domain	PD1PORT02	UP	UART0_RX	GPIO2				
CK Domain	PD1PORT03		UART0_TX	GPIO3				
CK Domain	PD1PORT04		OTP_AVDD_EN	GPIO4				
CK Domain	PD1PORT05	UP	SDBGTDI	DDBGTDI	SNDBGTDI	GPIO5		
CK Domain	PD1PORT06		SDBGTDO	DDBGTDO	SNDBGTDO	GPIO6		
CK Domain	PD1PORT07	UP	SDBGTMS	DDBGTMS	SNDBGTMS	PCM1INBCLK	GPIO7	
CK Domain	PD1PORT08	UP	SDBGTCK	DDBGTCK	SNDBGTCK	PCM1INLRCK	GPIO8	
CK Domain	PD1PORT09	UP	SDBGTRST	DDBGTRST	SNBGTRST	PCM1INDAT0	GPIO9	
CK Domain	PD1PORT11	UP	PCM1INBCLK	GPIO11				
CK Domain	PD1PORT12	UP	PCM1INLRCK	GPIO12				
CK Domain	PD1PORT13	UP	PCM1INDAT0	GPIO13				
CK Domain	PD1PORT14		PCMOUTMCLK	DUART_TX	GPIO14			
CK Domain	PD1PORT15		PCMOUTDAT0	SPDIF	GPIO15			
CK Domain	PD1PORT16		PCMOUTLRCK	GPIO16				
CK Domain	PD1PORT17		PCMOUTBCLK	GPIO17				
CK Domain	PD1PORT18	UP	UART1_RX	GPIO18				
CK Domain	PD1PORT19		UART1_TX	GPIO19				
CK Domain	PD1PORT20	UP	DDBGTDI	SNDBGTDI	GPIO20			
CK Domain	PD1PORT21	UP	DDBGTDO	SNDBGTDO	GPIO21			
CK Domain	PD1PORT22	UP	DDBGTMS	SNDBGTMS	GPIO22			
CK Domain	PD1PORT23	UP	DDBGTCK	SNDBGTCK	GPIO23			
CK Domain	PD1PORT24	UP	DDBGTRST	SNDBGTRST	GPIO24			
CK Domain	PD1PORT25		DUART_TX	SNUART_TX	GPIO25			

Domain	PORT_NAME	PULL	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3	FUNCTION4	FUNCTION5
CK Domain	PD1PORT26	UP	SDA0	GPIO26				
CK Domain	PD1PORT27	UP	SCL0	GPIO27				
CK Domain	PD1PORT28	UP	SDA1	GPIO28				
CK Domain	PD1PORT29	UP	SCL1	GPIO29				
CK Domain	PD1PORT30	UP	PCM0INDAT1	PDMDAT3	GPIO30			
CK Domain	PD1PORT31	UP	PCM0INDAT0	PDMDAT2	GPIO31			
CK Domain	PD1PORT32		PCM0INMCLK	PDMDAT1	GPIO32			
CK Domain	PD1PORT33	UP	PCM0INLRCK	PDMDAT0	PCM0OUTLRCK	GPIO33		
CK Domain	PD1PORT34	UP	PCM0INBCLK	PDMCLK	PCM0OUTBCLK	GPIO34		
CK Domain	PD1PORT35	UP	IR	GPIO35				
CK Domain	SPI0SCK		SPI0SCK					
CK Domain	SPI0MOSI	UP	SPI0MOSI					
CK Domain	SPI0CSn	UP	SPI0CSn					
CK Domain	SPI0MISO	UP	SPI0MISO					
ARM Domain	PD2PORT00	UP	BTDAT00	GPIO0				
ARM Domain	PD2PORT01	UP	BTDAT01	GPIO1				
ARM Domain	PD2PORT02	UP	BTDAT02	GPIO2				
ARM Domain	PD2PORT03	UP	BTDAT03	GPIO3				
ARM Domain	PD2PORT04	UP	BTCLK_IN	GPIO4				
ARM Domain	PD2PORT05		BT_RESET	GPIO5				
ARM Domain	PD2PORT06	UP	BTCLK_VSYNC	GPIO6				
ARM Domain	PD2PORT07	UP	BTCLK_HREF	GPIO7				
ARM Domain	PD2PORT08		BTCLK_OUT	GPIO8				
ARM Domain	PD2PORT09	UP	BTDAT04	SDA2	SPI1SCK	GPIO9		
ARM Domain	PD2PORT10	UP	BTDAT05	SCL2	SPI1MOSI	GPIO10		
ARM Domain	PD2PORT11	UP	BTDAT06	UART2_RX	SPI1CSn	GPIO11		
ARM Domain	PD2PORT12	UP	BTDAT07	UART2_TX	SPI1MISO	NUART_TX	AUART_TX	GPIO12

Domain	PORT_NAME	PULL	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3	FUNCTION4	FUNCTION5
ARM Domain	PD2PORT13	UP	BTDAT08	GPIO13				
ARM Domain	PD2PORT14	UP	BTDAT09	GPIO14				
ARM Domain	PD2PORT15	UP	BTDAT10	GPIO15				
ARM Domain	PD2PORT16	UP	BTDAT11	GPIO16				
ARM Domain	PD2PORT17	UP	BTDAT12	GPIO17				
ARM Domain	PD2PORT18	UP	BTDAT13	GPIO18				
ARM Domain	PD2PORT19	UP	BTDAT14	GPIO19				
ARM Domain	PD2PORT20	UP	BTDAT15	GPIO20				
ARM Domain	PD2PORT21	UP	UART3_RX	SD1CDn	SDA3	GPIO21		
ARM Domain	PD2PORT22		UART3_TX	SD1DAT1	SCL3	GPIO22		
ARM Domain	PD2PORT23	UP	DBGTDI	SD1DAT0	SPI2SCK	GPIO23		
ARM Domain	PD2PORT24		DBGTDO	SD1CLK	SPI2MOSI	GPIO24		
ARM Domain	PD2PORT25	UP	DBGTMS	SD1CMD	SPI2CSn	GPIO25		
ARM Domain	PD2PORT26	UP	DBGTCK	SD1DAT3	SPI2MISO	GPIO26		
ARM Domain	PD2PORT27	UP	DBGTRST	SD1DAT2	GPIO27			
ARM Domain	PD2PORT28	UP	UART2_RX	SDA2	GPIO28			
ARM Domain	PD2PORT29		UART2_TX	SCL2	GPIO29			
ARM Domain	PD2PORT30		SPI1SCK	NDBGTDI	ADBGTDI	GPIO30		
ARM Domain	PD2PORT31	UP	SPI1MOSI	NDBGTDO	ADBGTDO	GPIO31		
ARM Domain	PD2PORT32		SPI1CSn	NDBGTMS	ADBGTMS	GPIO32		
ARM Domain	PD2PORT33	UP	SPI1MISO	NDBGTCK	ADBGTCK	GPIO33		
ARM Domain	PD2PORT34	UP	SPI2SCK	NDBGTRST	ADBGTRST	GPIO34		
ARM Domain	PD2PORT35	UP	SPI2MOSI	GPIO35				
ARM Domain	PD2PORT36	UP	SPI2CSn	GPIO36				
ARM Domain	PD2PORT37	UP	SPI2MISO	GPIO37				
ARM Domain	PD2PORT38	UP	SD0CDn	GPIO38				
ARM Domain	PD2PORT39	UP	SD0DAT1	GPIO39				

Domain	PORT_NAME	PULL	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3	FUNCTION4	FUNCTION5
ARM Domain	PD2PORT40	UP	SD0DAT0	GPIO40				
ARM Domain	PD2PORT41		SD0CLK	GPIO41				
ARM Domain	PD2PORT42	UP	SD0CMD	GPIO42				
ARM Domain	PD2PORT43	UP	SD0DAT3	GPIO43				
ARM Domain	PD2PORT44	UP	SD0DAT2	GPIO44				
ARM Domain	PD2PORT45	UP	SD1CDn	GPIO45				
ARM Domain	PD2PORT46	UP	SD1DAT1	GPIO46				
ARM Domain	PD2PORT47	UP	SD1DAT0	GPIO47				
ARM Domain	PD2PORT48		SD1CLK	GPIO48				
ARM Domain	PD2PORT49	UP	SD1CMD	GPIO49				
ARM Domain	PD2PORT50	UP	SD1DAT3	GPIO50				
ARM Domain	PD2PORT51	UP	SD1DAT2	GPIO51				

4.4. CK Domain Power and Ground Pins

Table 4-2 Power and Ground Pins

Pin Number	Signal	Type	Description
K12,F12	PD1VDD33	DP	3.3V digital power for IO
L11,K11，L12,J12，H12,G12	PD1VDD11	DP	1.1V digital power for core
D12	ADACVDD33	AP	Power (3.3V) for Audio DAC
D10	EFUSEVDD25	AP	Power (2.5V) for EFUSE
D11	AADCVDD33	AP	Power (3.3V) for Audio ADC
D09	LDO25CMP	AP	Power (2.5V) for ADC power compensate
M11	PD1USBAVDD33	AP	Power (3.3V) for USB Slave

Pin Number	Signal	Type	Description
M12	PD1USBAVDD11	AP	Power (1.1V) for USB Slave
N10,M05,M07,L04,L08,L10,K03,K06,K07,K08,K09,K10,J07,J08,J09,J10,J11,H03,H06,H07,H08,H09,H10,H11,G06,G07,G08,G09,G10,G11,F03,F05,F06,F07,F08,F09,F10,F11,E06,E07,E08,E09,E10,E11,E12,D05,D08	GND	DG/AG	GND

4.5. CK Domain System Operation Pins

Table 4-3 System Operation Pins

Pin Number	Signal	Type	Description
H15	XIN	I	Clock input or crystal input
H14	XOUT	O	Output for crystal connection
G13	RSTn	I	System reset, active low

4.6. CK Domain ADC Interface Signals

Table 4-4 ADC Interface Signal Pins

Pin Number	Signal	Type	Description
C12	BIAS0	AO	Bias Voltage, Channel 0

Pin Number	Signal	Type	Description
A13	AIN0N	AI	Differential Voltage Inputs, Channel 0
B13	AIN0P	AI	Differential Voltage Inputs, Channel 0
C11	BIAS1	AO	Bias Voltage, Channel 1
A12	AIN1N	AI	Differential Voltage Inputs, Channel 1
B12	AIN1P	AI	Differential Voltage Inputs, Channel 1
C10	BIAS2	AO	Bias Voltage, Channel 2
A10	AIN2N	AI	Differential Voltage Inputs, Channel 2
B11	AIN2P	AI	Differential Voltage Inputs, Channel 2
C09	BIAS3	AO	Bias Voltage, Channel 3
B09	AIN3N	AI	Differential Voltage Inputs, Channel 3
B10	AIN3P	AI	Differential Voltage Inputs, Channel 3
C08	BIAS4	AO	Bias Voltage, Channel 4
B08	AIN4N	AI	Differential Voltage Inputs, Channel 4
A08	AIN4P	AI	Differential Voltage Inputs, Channel 4
D07	BIAS5	AO	Bias Voltage, Channel 5
B07	AIN5N	AI	Differential Voltage Inputs, Channel 5
C07	AIN5P	AI	Differential Voltage Inputs, Channel 5
C06	BIAS6	AO	Bias Voltage, Channel 6
A06	AIN6N	AI	Differential Voltage Inputs, Channel 6
B06	AIN6P	AI	Differential Voltage Inputs, Channel 6

Pin Number	Signal	Type	Description
D06	BIAS7	AO	Bias Voltage, Channel 7
B05	AIN7N	AI	Differential Voltage Inputs, Channel 7
C05	AIN7P	AI	Differential Voltage Inputs, Channel 7

4.7. CK Domain SPI Flash Signals

Table 4-5 Flash Signals

Pin Number	Signal	Type	Description
G14	SPI0SCK	O	SCK of SPI interface
F13	SPI0MOSI	O	MOSI of SPI interface
F15	SPI0CSn	O	CS of SPI interface
F14	SPI0MISO	I	MISO of SPI interface

4.8. CK Domain Audio Play Interface Signals

Table 4-6 Audio Paly Interface Signals

Pin Number	Signal	Type	Description
A15	AOR	AO	Audio DAC right channel output
A14	AOL	AO	Audio DAC left channel output
M13	PCMOUTMCLK	O	0: mclk of audio out i2s interface
	DUARTTX	O	1: DSP UART data transmit
	SNUARTTX	O	2: SNPU UART data transmit

Pin Number	Signal	Type	Description
M13	PD1PORT14	IO	3: Domain1 GPIO 14
N15	PCMOUTDAT0	O	0: data0 of audio out I2S interface
	SPDIF	O	1: Sony/Philips Digital Interface Format
	PD1PORT15	IO	2: Domain1 GPIO 15
M14	PCMOUTLRCK	O	0: lrclk of audio in0 i2s interface
	PD1PORT16	IO	1: Domain1 GPIO 16
M15	PCMOUTBCLK	O	0: bclk of audio out i2s interface
	PD1PORT17	IO	1: Domain1 GPIO 17

4.9. CK Domain Communication Interface Signals

Table 4-7 Communication Interface Signals

Pin Number	Signal	Type	Description
D13	SDA1	IO	0: Data of I2C 1
	PD1PORT28	IO	1: Domain1 GPIO 28
D14	SCL1	IO	0: Clock of I2C 1
	PD1PORT29	IO	1: Domain1 GPIO 29
N11	UART0TX	O	0: UART0 data transmit
	PD1PORT03	IO	1: Domain1 GPIO 03
P11	UART0RX	I	0:UART0 data receive
	PD1PORT02	IO	1: Domain1 GPIO 02

Pin Number	Signal	Type	Description
N12	POWER_DOWN	O	0: CK Domain Power_down Controller
	PD1PORT01	IO	1: Domain1 GPIO 01
P12	BOOT	I	0: Boot key
	PD1PORT00	IO	1: Domain1 GPIO 00
E13	SDA0	IO	0: Data of I2C 0
	PD1PORT26	IO	1: Domain1 GPIO 26
E14	SCL0	IO	0: Clock of I2C 0
	PD1PORT27	IO	1: Domain1 GPIO 27
L14	UART1TX	O	0: UART1 data transmit
	PD1PORT19	IO	1: Domain1 GPIO 19
L13	UART1RX	I	0:UART1 data receive
	PD1PORT18	IO	1: Domain1 GPIO 18
B14	IR	I	0:Infrared reception
	PD1PORT35	IO	1: Domain1 GPIO 35
H13	DUARTTX	O	0: DSP UART data transmit
	SNUARTTX	O	1: SNPU UART data transmit
	PD1PORT25	IO	2: Domain1 GPIO 25
R12	OTP_AVDD_EN	I	0:OTP VDD EN
	PD1PORT04	IO	1: Domain1 GPIO 04

4.10.CK Domain ECHO Interface Signals

Table 4-8 Audio In Interface Signals

Pin Number	Signal	Type	Description
N14	PCM1INDAT0	I	0: data0 of audio in0 i2s interface
	PD1PORT13	IO	1: Domain1 GPIO 13
R15	PCM1INLRCK	I	0: clk of audio in0 i2s interface
	PD1PORT12	IO	1: Domain1 GPIO 12
P15	PCM1INBCLK	I	0: bclk of audio out i2s interface
	PD1PORT11	IO	1: Domain1 GPIO 11

4.11.CK Domain Audio In Interface Signals

Table 4-9 USB Interface Signals

Pin Number	Signal	Type	Description
C14	PCM0INDAT0	I	0: data0 of audio in0 i2s interface
	PDMDAT2	I	1: data2 of audio in pdm interface
	PD1PORT31	IO	2: Domain1 GPIO 31
C15	PCM0INMCLK	I	0: mclk of audio in0 i2s interface
	PDMDAT1	I	1: data1 of audio in pdm interface
	PD1PORT32	IO	2: Domain1 GPIO 32
C13	PCM0INLRCK	I	0: lrck of audio in0 i2s interface
	PDMDAT0	I	1: data0 of audio in pdm interface

Pin Number	Signal	Type	Description
C13	PCM0OUTLRCK	O	2: lrck of audio out i2s interface from core
	PD1PORT33	IO	3: Domain1 GPIO 33
B15	PCM0INBCLK	I	0: bclk of audio in0 i2s interface
	PDMCLK	O	1: mclk of audio in pdm interface
	PCM0OUTBCLK	O	2: bclk of audio out i2s interface from core
	PD1PORT34	IO	3: Domain1 GPIO 34
D15	PCM0INDAT1	I	0: data1 of audio in0 i2s interface
	PDMDAT3	I	1: data3 of audio in pdm interface
	PD1PORT30	IO	2: Domain1 GPIO 30

4.12.CK Domain USB Slave Interface Signals

Table 4-10 USB Slave Interface Signals

Pin number	Signal	Type	Description
R10	PD1USBDP	AB	USB Slave Data pin Data+
P10	PD1USBDM	AB	USB Slave Data pin Data-

4.13.CK Domain JTAG Interface Signals

Table 4-11 JTAG Interface Signals

Pin Number	Signal	Type	Description
P13	SDBGTDI	I	0: SCPU Debug interface data input

Pin Number	Signal	Type	Description
P13	PD1PORT05	IO	1: Domain1 GPIO 05
R13	SDBGTDO	O	0: SCPU Debug interface data ouput
	PD1PORT06	IO	1 Domain2 GPIO 06
N13	SDBGTMS	I	0: SCPU Debug interface mode select
	PD1PORT07	IO	1: Domain 1 GPIO 07
R14	SDBGTCK	I	0: SCPU Debug interface clock
	PD1PORT08	IO	1: Domain 1 GPIO 08
P14	SDBGTRST	I	0: SCPU Debug interface reset
	PD1PORT09	IO	1: Domain 1 GPIO 09
K14	DDBGTDI	I	0: DSP Debug interface data input
	SNDBGTDI	I	1: SNPU Debug interface data input
	PD1PORT20	IO	2: Domain1 GPIO 20
K13	DDBGTDO	O	0: DSP Debug interface data ouput
	SNDBGTDO	O	1: SNPU Debug interface data ouput
	PD1PORT21	IO	2: Domain2 GPIO 21
K15	DDBGTMS	I	0: DSP Debug interface mode select
	SNDBGTMS	I	1: SNPU Debug interface mode select
	PD1PORT22	IO	2: Domain 1 GPIO 22

Pin Number	Signal	Type	Description
J14	DDBGTCK	I	0: DSP Debug interface clock
	SNDBGTCK	I	1: SNPU Debug interface clock
	PD1PORT23	IO	2: Domain 1 GPIO 23
J13	DDBGTRST	I	0: DSP Debug interface reset
	SNDBGTRST	I	1: SNPU Debug interface reset
	PD1PORT24	IO	2: Domain 1 GPIO 24

4.14.ARM Domain Power and Ground Pins

Table 4-12 Power and Ground Pins

Pin Number	Signal	Type	Description
M06,E04	PD2VDD33	DP	3.3V digital power for IO
M04,M08,L05,L06,L07,L09,K05,J06,H05,G04,F04,H02	PD2VDD11	DP	1.1V digital power for core
K04,J05,H04,G05,E05	VDDP15_DDR	AP	Power (1.5V) for DDR3
J04	VREF	AP	Power (0.75V) for DDR REF
M09	PD2USBAVDD33	AP	Power (3.3V) for USB Host
M10	PD2USBAVDD11	AP	Power (1.1V) for USB Host
D04	PD2BTVDD30	DP	Power (3.0V) for bt1120

4.15.ARM Domain Communication Interface Signals

Table 4-13 Communication Interface Signals

Pin Number	Signal	Type	Description
M01	UART2RX	I	0: UART2 data receive
	SDA2	IO	1: Data of I2C 2
	PD2PORT28	IO	2: Domain 2 GPIO 28
M02	UART2TX	O	0: UART2 data transmit
	SCL2	IO	1: Clock of I2C 2
	PD2PORT29	IO	2: Domain 2 GPIO 29
J02	UART3RX	I	0: UART3 data receive
	SDA3	IO	2: Data of I2C 3
	PD2PORT21	IO	3: Domain 2 GPIO 21
J01	UART3TX	O	0: UART3 data transmit
	SCL3	IO	2: Clock of I2C 3
	PD2PORT22	IO	3: Domain 2 GPIO 22

4.16.ARM Domain USB Interface Signals

Table 4-14 USB Interface Signals

Pin Number	Signal	Type	Description
N09	PD2USBDP	AB	USB Host Data pin Data+
P09	PD2USBDM	AB	USB Host Data pin Data-

4.17.ARM Domain SPI Interface Signals

Table 4-15 USB Interface Signals

Pin Number	Signal	Type	Description
N01	SPI1SCK	O	0:SCK of SPI interface 1
	NDBGTDI	I	1: NPU Debug interface data input
	ADBGTDI	I	2: Audio Debug interface data input
	PD2PORT30	IO	3: Domain 2 GPIO 30
M03	SPI1MOSI	O	0: MOSI of SPI interface 1
	NDBGTDO	O	1: NPU Debug interface data ouput
	ADBGTDO	O	2: Audio OR Debug interface data ouput
	PD2PORT31	IO	3: Domain 2 GPIO 31
P01	SPI1CSn	O	0:CSn of SPI interface 1
	NDBGTMS	I	1: NPU Debug interface mode select
	ADBGTMS	I	2: Audio OR Debug interface mode select
	PD2PORT32	IO	3: Domain 2 GPIO 32
N02	SPI1MISO	I	0:MISO of SPI interface 1
	NDBGTCK	I	1: NPU Debug interface clock
	ADBGTCK	I	2: Audio OR Debug interface clock
	PD2PORT33	IO	3: Domain 2 GPIO 33
P02	SPI2SCK	I	0:SCK of SPI interface 2
	NDBGTRST	I	1: NPU Debug interface reset
	ADBGTRST	I	2: Audio OR Debug interface reset

Pin Number	Signal	Type	Description
	PD2PORT34	IO	3: Domain 2 GPIO 34
P03	SPI2MOSI	I	0:MOSI of SPI interface 2
	PD2PORT35	IO	1: Domain 2 GPIO 35
R02	SPI2CSn	I	0:CSn of SPI interface 2
	PD2PORT36	IO	1: Domain 2 GPIO 36
N03	SPI2MISO	O	0:MISO of SPI interface 2
	PD2PORT37	IO	1: Domain 2 GPIO 37

4.18.ARM Domain JTAG Interface Signals

Table 4-16 JTAG Interface Signals

Pin Number	Signal	Type	Description
J03	DBGTDI	I	0: ARM Debug interface data input
	PD2PORT23	IO	1: Domain 2 GPIO 23
K01	DBGTDO	O	0: ARM Debug interface data output
	PD2PORT24	IO	1: Domain 2 GPIO 24
K02	DBGTMS	I	0: ARM Debug interface mode select
	PD2PORT25	IO	1: Domain 2 GPIO 25
L02	DBGTCK	I	0: ARM Debug interface clock
	PD2PORT26	IO	1: Domain 2 GPIO 26
L03	DBGTRST	I	0: ARM Debug interface reset

Pin Number	Signal	Type	Description
	PD2PORT27	IO	1: Domain 2 GPIO 27

4.19.ARM Domain SDIO Interface Signals

Table 4-17 SDIO Interface Signals

Pin Number	Signal	Type	Description
N04	SD0CDn	I	0: Card Detect of SDIO Interface 0
	PD2PORT38	IO	1: Domain 2 GPIO 38
P04	SD0DAT1	IO	0: Data Line 1 of SDIO Interface 0
	PD2PORT39	IO	1: Domain 2 GPIO 39
R04	SD0DAT0	IO	0: Data Line 0 of SDIO Interface 0
	PD2PORT40	IO	1: Domain 2 GPIO 40
N05	SD0CLK	O	0: Clock of SDIO Interface 0
	PD2PORT41	IO	1: Domain 2 GPIO 41
R05	SD0CMD	IO	0: Command of SDIO Interface 0
	PD2PORT42	IO	1: Domain 2 GPIO 42
P05	SD0DAT3	IO	0: Data Line 3 of SDIO Interface 0
	PD2PORT43	IO	1: Domain 2 GPIO 43
P06	SD0DAT2	IO	0: Data Line 2 of SDIO Interface 0
	PD2PORT44	IO	1: Domain 2 GPIO 44
N06	SD1CDn	I	0: Card Detect of SDIO Interface 1

Pin Number	Signal	Type	Description
	PD2PORT45	IO	1: Domain 2 GPIO 45
P07	SD1DAT1	IO	0: Data Line 1 of SDIO Interface 1
	PD2PORT46	IO	1: Domain 2 GPIO 46
N07	SD1DAT0	IO	0: Data Line 0 of SDIO Interface 1
	PD2PORT47	IO	1: Domain 2 GPIO 47
R07	SD1CLK	O	0: Clock of SDIO Interface 1
	PD2PORT48	IO	1: Domain 2 GPIO 48
P08	SD1CMD	IO	0: Command of SDIO Interface 1
	PD2PORT49	IO	1: Domain 2 GPIO 49
R08	SD1DAT3	IO	0: Data Line 3 of SDIO Interface 1
	PD2PORT50	IO	1: Domain 2 GPIO 50
N08	SD1DAT2	IO	0: Data Line 2 of SDIO Interface 1
	PD2PORT51	IO	1: Domain 2 GPIO 51

4.20.ARM Domain BT1120 Interface Signals

Table 4-18 BT1120 Interface Signals

Pin Number	Signal	Type	Description
A04	BTDAT00	I	0: Data 00 of Bt1120 Interface
	PD2PORT00	IO	1: Domain 2 GPIO 00
A02	BTDAT01	I	0: Data 01 of Bt1120 Interface

Pin Number	Signal	Type	Description
	PD2PORT01	IO	1: Domain 2 GPIO 01
A03	BTDAT02	I	0: Data 02 of Bt1120 Interface
	PD2PORT02	IO	1: Domain 2 GPIO 02
B04	BTDAT03	I	0: Data 03 of Bt1120 Interface
	PD2PORT03	IO	1: Domain 2 GPIO 03
A01	BTCLK_IN	I	0: Clock in of Bt1120 Interface
	PD2PORT04	IO	1: Domain 2 GPIO 04
C04	BT_RESET	O	0: Reset of Bt1120 Interface
	PD2PORT05	IO	1: Domain 2 GPIO 05
B02	BTCLK_VSYNC	I	0: VSYNC of Bt1120 Interface
	PD2PORT06	IO	1: Domain 2 GPIO 06
B03	BTCLK_HREF	I	0: HREF of Bt1120 Interface
	PD2PORT07	IO	1: Domain 2 GPIO 07
B01	BTCLK_OUT	O	0: clock out of Bt1120 Interface
	PD2PORT08	IO	1: Domain 2 GPIO 08
C01	BTDAT04	I	0: Data 04 of Bt1120 Interface
	PD2PORT09	IO	1: Domain 2 GPIO 09
C02	BTDAT05	I	0: Data 05 of Bt1120 Interface
	PD2PORT10	IO	1: Domain 2 GPIO 10
D01	BTDAT06	I	0: Data 06 of Bt1120 Interface

Pin Number	Signal	Type	Description
	PD2PORT11	IO	1: Domain 2 GPIO 11
C03	BTDAT07	I	0: Data 07 of Bt1120 Interface
	PD2PORT12	IO	1: Domain 2 GPIO 12
	NUARTTX	O	2: NPU UART data transmit
	AUARTTX	O	3: Audio OR UART data transmit
D02	BTDAT08	I	0: Data 08 of Bt1120 Interface
	PD2PORT13	IO	1: Domain 2 GPIO 13
D03	BTDAT09	I	0: Data 09 of Bt1120 Interface
	PD2PORT14	IO	1: Domain 2 GPIO 14
E02	BTDAT10	I	0: Data 10 of Bt1120 Interface
	PD2PORT15	IO	1: Domain 2 GPIO 15
E03	BTDAT11	I	0: Data 11 of Bt1120 Interface
	PD2PORT16	IO	1: Domain 2 GPIO 16
F01	BTDAT12	I	0: Data 12 of Bt1120 Interface
	PD2PORT17	IO	1: Domain 2 GPIO 17
G01	BTDAT13	I	0: Data 13 of Bt1120 Interface
	PD2PORT18	IO	1: Domain 2 GPIO 18
F02	BTDAT14	I	0: Data 14 of Bt1120 Interface
	PD2PORT19	IO	1: Domain 2 GPIO 19
G02	BTDAT15	I	0: Data 15 of Bt1120 Interface

Pin Number	Signal	Type	Description
	PD2PORT20	IO	1: Domain 2 GPIO 20

5. Applications

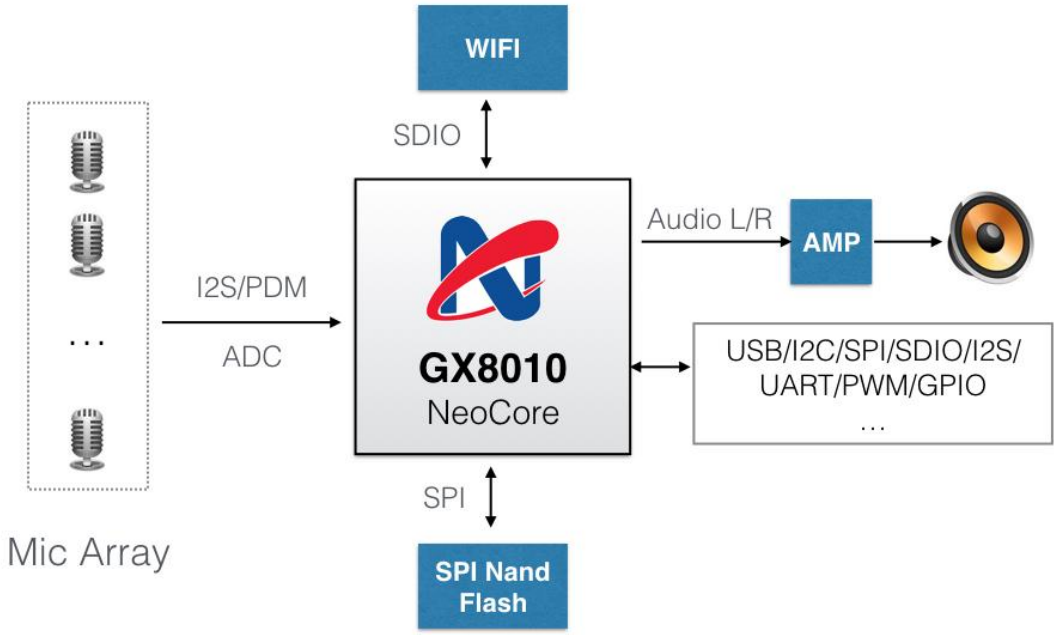


Figure 5-1 Classic GX8010 Application Diagram

6. Electronic Specification

6.1. Recommended operating conditions

Table 6-1 Recommended operating conditions

Parameters	Min	Typ	Max	Units
Output High Level (VOH)	2.4	2.8	3.3	V
Output Low Level (VOL)	0	0.2	0.4	V
Input High Level (VIH)	2.0	2.8	3.6	V
Input Low Level (VIL)	-0.3	0	0.8	V
Low Level Output Current@VOL(IOL)			9.5	mA
High Level Output Current@VOH(IOH)			26.5	mA
Input Leakage Current(II)			-10	μA
Pull-up Resistor	58	86	133	kΩ
Pull-down Resistor	52	78	128	kΩ
Storage Temperature	-40		150	℃
Operating Ambient Temperature	-20	30	95	℃
Thermal Resistance		32		℃

6.2. Electronic Characteristics of CK Domain

Table 6-2 Electronic characteristics of CK Domain

Parameters	Min	Typ	Max	Units
1.1V Power Supply Voltage	1.05	1.10	1.21	V

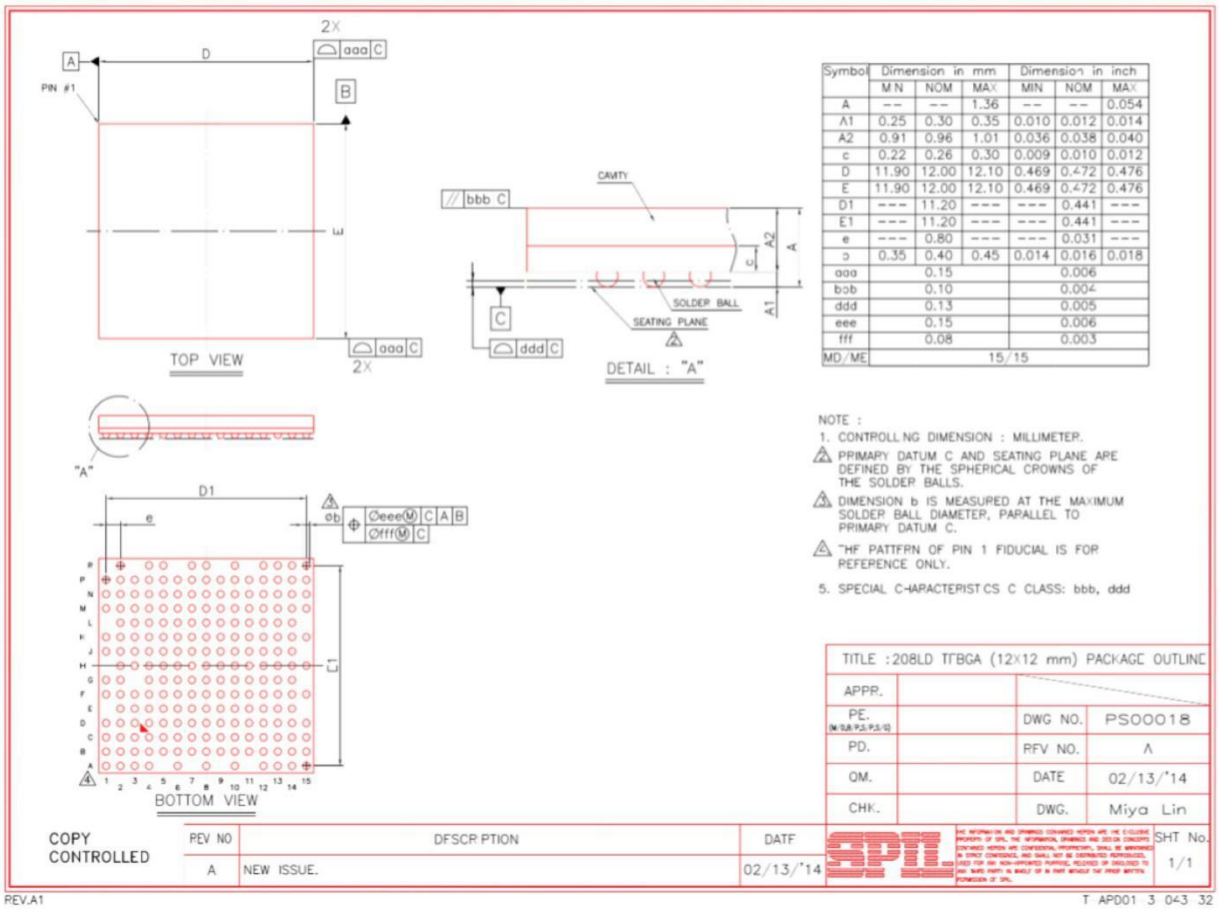
Parameters	Min	Typ	Max	Units
1.1V Power Supply Current	20	200	250	mA
2.5V Power Supply Voltage	2.25	2.5	2.75	V
2.5V Power Supply Current	4.5	5	5.5	mA
3.3V Digital Power Supply Voltage	2.8	3.3	3.6	V
3.3V Digital Power Supply Current	10	15	20	mA
3.3V Analog Power Supply Voltage	2.8	3.3	3.6	V
3.3V Analog Power Supply Current	2.25	11.25	22.5	mA
Leakage Current	15	24	28	mA

6.3. Electronic Characteristics of ARM Domain

Table 6-3 Electronic Characteristics of ARM Domain

Parameters	Min	Typ	Max	Units
1.1V Power Supply Voltage	1.05	1.10	1.21	V
1.1V Power Supply Current	55	380	500	mA
1.5V Power Supply Voltage	1.35	1.5	1.65	V
1.5V Power Supply Current	10	80	130	mA
3.3V Digital Power Supply Voltage	2.8	3.3	3.6	V
3.3V Digital Power Supply Current	10	15	20	mA
Leakage Current	32	40	50	mA

7. Package Information



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.36	--	--	0.054
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	11.90	12.00	12.10	0.469	0.472	0.476
E	11.90	12.00	12.10	0.469	0.472	0.476
D1	---	11.20	---	---	0.441	---
E1	---	11.20	---	---	0.441	---
e	---	0.80	---	---	0.031	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.13			0.005	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME		15/15				

REV NO	DESCRIPTION	DATE
A	NEW ISSUE.	02/13/'14

Figure: 7-1 TFBGA208 Package parameters

8. Ordering Information

Table 8-1 GX8010 Ordering Information

Ordering Code	Embedded DDR	Package
GX8010A	128M bytes	TFBGA208
GX8010B	256M bytes	TFBGA208

Revision History:

Version	Time	Change Log	Author
V0.1	2017.7.2	Initial version	Robot.Ling
V0.2	2017.7.12	Fixed some minor mistake	Robot.Ling
v0.3	2017.8.7	Fixed the standby power description	Robot.Ling
v0.5	2017.11.15	Fixed DAC description	Robot.Ling
V1.0	2017.11.24	Fixed Pin map and description	Lin Jing
V1.1	2017.12.04	Fixed some minor mistake	Lin Jing
V1.2	2017.12.29	Fixed Pin map	Lin Jing
V1.3	2018.03.02	Fixed some detailed data	Lin Jing
V1.4	2018.05.25	Added pin mux	Lin Jing
V1.5	2018.06.29	Fixed some minor data	Lin Jing
V1.6	2018.11.19	Fixed electronic specification	Lin Jing
V1.7	2019.09.24	Fixed electronic specification	Lin Jing
V1.8	2019.12.11	Fixed some description	Lin Jing

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